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ARM Processor Architecture: An Emerging Architecture in Smart Phones

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Abstract

ARM is a 32-bit RISC processor architecture. It is develop and licenses by British company ARM holdings. ARM holding does not manufacture and sell the CPU devices. ARM holding only licenses the processor architecture to interested parties. There are two main types of licences implementation licenses and architecture licenses. ARM processors have a unique combination of feature such as ARM core is very simple as compare to general purpose processors. ARM chip has several peripheral controller, a digital signal processor and ARM core. ARM processor consumes less power but provide the high performance. Now a day, ARM Cortex series is very popular in Smartphone devices. We will also see the important characteristics of cortex series. We discuss the ARM processor and system on a chip (SOC) which includes the Qualcomm, Snapdragon, nVidia Tegra, and Apple system on chips. In this paper, we discuss the features of ARM processor and Intel atom processor and see which processor is best. Finally, we will discuss the future of ARM processor in Smartphone devices.

Keywords

RISC, ISA, ARM Core, System on a Chip (SoC)

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1. Introduction

ARM is a 32 bit RISC processor. ARM processor is designed and licensed by British company ARM holding. It is develop in 1980's by Acorn Computers Ltd. Its old name was an acronym for Acorn RISC Machine. Now its new name is an Advanced RISC Machine. In 2013 ARM is a mostly widely used 32-bit instruction set architecture. In 2010 ARM processors reported the shipments of 6.1 billion, represents the 95% of smart phone, 35% of digital televisions and 10% of mobile computers.

Design of ARM processor is very simple and covers very less space as compare to powerful RISC machine. ARM's goal is to optimize the price and performance ratio rather than building the most powerful processor in the market. Assembling of ARM processor takes a very less time. As we know that chip is very small and CMOS technology make this processor energy efficient. ARM processors have the ability to shutdown the clock automatically that's why it is very popular in embedded applications. [2]

ARM holding does not manufacture the electronic chips but only provide the licenses and design to other semiconductor manufactures. ARM processor and system on chip (SoC) include the QualComm, Snapdragon, nVidia Tegra, and Apple system on chip. ARM offers the different licensing terms which are varying in cost. [7]

ARM provides the complete software development toolkit and sells the Silicon containing chip the ARM CPU. There are two main types of licenses implementation licenses and architecture licenses integrated circuit containing an ARM processor core, while the architecture licenses develop their own processor with ARM ISA.

ARM processor has a unique combination of features which makes the ARM processor very popular in embedded architecture. ARM processor core is very simple as compare to general purpose processors. ARM uses a very less number

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of transistors. ARM chip can contain several peripheral controllers, digital signal processor, very little memory on chip and ARM core.

ISA and pipeline are used to minimize the energy which is requiring in mobile embedded systems. ARM processor has a load and store ISA. Most of the processors use a 3-stage pipeline consisting of fetch, decode and execution stages. The pipeline executes one instruction per cycle.

The ARM processor designs are using custom standard cells. The ARM architecture is a modular, the main important component of an ARM processor is an integer pipeline while the other components caches, MMU, floating point and coprocessors are optional.

Thumb mode uses a 16 bit instruction to reduce the code density. This increase the performance of the processor where

smaller memory and data buses are used. Some new processors allow Java byte code execution directly from ARM pipeline called Jazelle.

ARM can extend the instruction set when coprocessor is added. [2]

In the end we compare the features of ARM and Intel atom processors. We also see the 64-bit ARM processor and the future of ARM processor. [11]

2. REVIEW and Related Work

The ARM started his work in 1983 when a company Acorn computer was searching a 16 bit microprocessor for their next desktop machine. Early microprocessors did not cover their requirements. These parts are slower than standard parts available at that time. At that time CISC was taking hundred of cycles to execute.

Therefore Acorn engineers decided to design their own microprocessor. After two years, the Berkeley RISC 1 project builds a very simple microprocessor. Acorn decided to pick up this Berkeley approach and launch their 26 bit Acorn RISC Machine in 1985. The first ARM processor is called as the ARM version 1 architecture. In 1992 a new, ARM included the coprocessor support feature.

Later, ARM v2 architecture included the on-chip cache in ARM3 processor. In 1990 Apple decided to use the ARM processor in Newton PDA. A joint venture by Acorn and Apple to design a new processor; now, the new name is the ARM, which stands for Advanced RISC machine. Third version of ARM architecture was consisting of 32 bit addressing; MMU and 64 bit multiply accumulate instructions. The release of ARM 6 and ARM 7 processors and Newton PDA moved to the embedded market.

In 1996 ARM cores v4 was support for Thumb 16-bit compressed instruction set. Thumb code takes 40% less space compared to regular 32-bit while ARM code is a little less efficient. The most popular ARM cores v4 is the ARM7TDMI core, which is the most popular ARM product. This is used in most Apple iPod players, including the video iPod.

In 1999, ARM v5 architecture introduced digital signal processing and Java byte code extensions to the ARM instruction set. The most popular implementation of this architecture is the Intel X-Scale processor.

The 6th generation of the ARM architecture released in 2001, which introduce SIMD instruction set extension, improved Thumb instruction set, the Trust Zone virtualisation technology, and multiprocessor support.

The newly released ARMv7 architecture extended SIMD instructions set and improved floating point support. [2]

Table 1. The history of ARM Processor.

Version	Features	Implementations
v1	The first commercial RISC (26-bit)	ARM 1
v2	Coprocessor support	ARM 2, ARM 3
v3	32-bit, MMU, 64-bit MAC	ARM 6, ARM 7
v4	Thumb	ARM7TDMI, ARM8, ARM9TDMI, Strong ARM
v5	DSP and Jazelle extensions	ARM10, XScale
v6	SIMD, Thumb-2, Trust-Zone, multiprocessing	ARM11, ARM11 MPCore

3. World of ARM

ARM lies at the heart of digital products, mobile phone, digital camera and automotive system. ARM is a leading intellectual property (IP) of high performance, low cost, power efficient and system on chip (SOC) designs with the different organizations. ARM architecture is compatible with all major operating systems such as Symbian OS, Palm OS, LINUX and Windows CE. ARM also provides the software solutions to existing market segments.

These benefits are making ARM company a complete solution provider. There are above the forty parterres which use the ARM licences. ARM enables original equipment manufacturers (OEM) which recognize accelerated time to

market through complete product offerings. These are Prime Cell Peripherals, embedded software IP, development tools, training, and support.

ARM's Global Technology Partner Network is the largest in the industry, spanning from semiconductor manufacturers to distributors.

ARM ensure that the partnership provide the solutions in real time operating systems, development systems, application software and design consulting. [5]

4. Design of ARM Architecture

The design of ARM processor architecture pass through many steps until it reaches the final form. The ARM processor is constructed from the following components Arithmetic Logic Unit, Booth multiplier, Barrel shifter and control unit. We will discuss these components:

1. In ALU, the ALU has two 32 bit inputs. The first input comes from the register file and second input comes from the shifter. Actually, ALU change the output of status register flags.
2. In Booth multiplexer, the multiplexer has three 32 bits inputs. While, all the inputs come from the register file. So, the output of multiplier is only the 32 least significant bits of the product. This multiplication starts when we start the input goes active.
3. In Barrel shifter, the Barrel shifter shifts the 32 bit input. This input comes from the register file. This is may be the immediate data. The shifter have other control inputs which comes from the instruction register (IR). While, the shift field in the instruction can control the operation of Barrel shifter. This field represents the type of shift which is to be performed. The possible type of shift is logical left or right, arithmetic right or rotates right.
4. In control unit, control unit is the heart of microprocessor. This is responsible for the system operation. So, control unit is a pure combinational circuit. In our design, control unit is implemented by simple state machine. The processor timing is also included in the control unit. Signals from the control unit are connected to every component in the processor to supervise its operation.

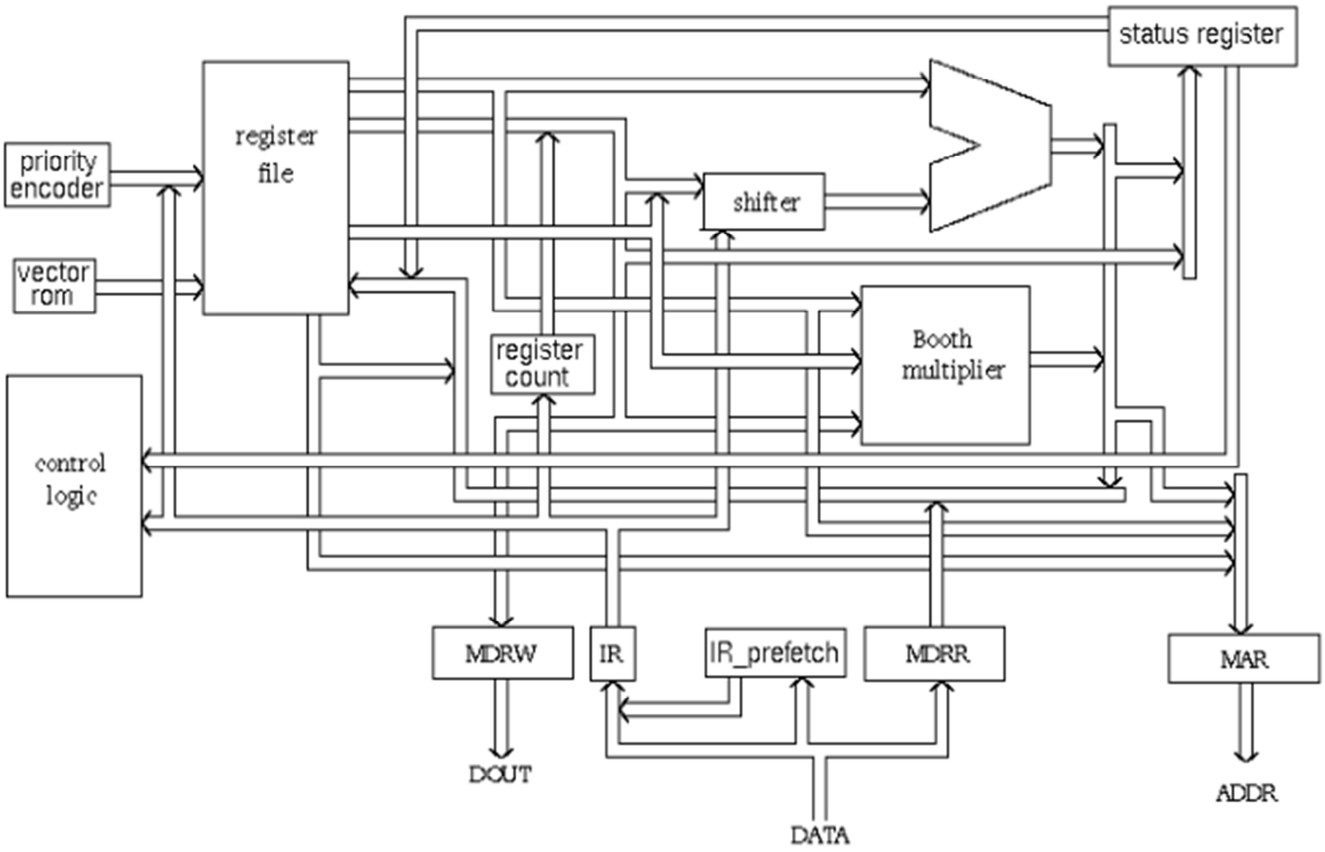

Figure 1. ARM block diagram [3].

The ARM processor also includes the other components:

1. Program status register contains the processor flags (z, s, v and c). In this register, we have the mode bits with the interrupt and fast interrupt disable bits.
2. Some special registers use the instruction register, memory data read/write register and memory address register. While the priority encoder use in the multiple load/store instruction. This show that which registers is use in the register file to be load/store.

The multiplexer's are used to control the operation of processor buses. We represent these components in a behavioural model. Every component is representing with an entity.

This made the design easier to construct and maintain [3].

4.1. Explanation of ARM Architecture

ARM cores use 32 bit load/store RISC architecture. The core cannot directly manipulate the memory. The data manipulation can be done by loading registers. This performs the data operation and then stores the value back to memory. There are 37 registers in the processor. So, there are seven different modes of processor. These processor modes are run at user tasks, an operating system and interrupts. While, some of the registers are reserve for specific use with the core and mostly are available for general use. The reserve registers use the r13 as the stack pointer (SP), r14 as a link register (LR),

r15 as a program counter (PC), the current status register (CPSR) and saved program status register (SPSR).

The SPSR and CPSR contain the status and control bits. This specifies the properties of the processor core are operating order. Hence, these properties define the operating mode, ALU status flags, interrupt disable and enable flags.

We divide the 37 total registers among the seven processor modes. The above figure shows that the bank of registers visible in each mode.

1. User mode is only non-privileged mode. This holds a least number of total registers visible. In this mode most of the application and OS task run.
2. In FIQ mode, entered when a high priority (fast) interrupt is raised.
3. In IRQ mode, entered when a low priority (normal) interrupt is raised.
4. In SVC mode, this is the default mode of processor on start up or reset.
5. In Un-def mode, this is use to handle the undefined instructions.
6. In Abort mode, this mode is use to handle memory access violations.

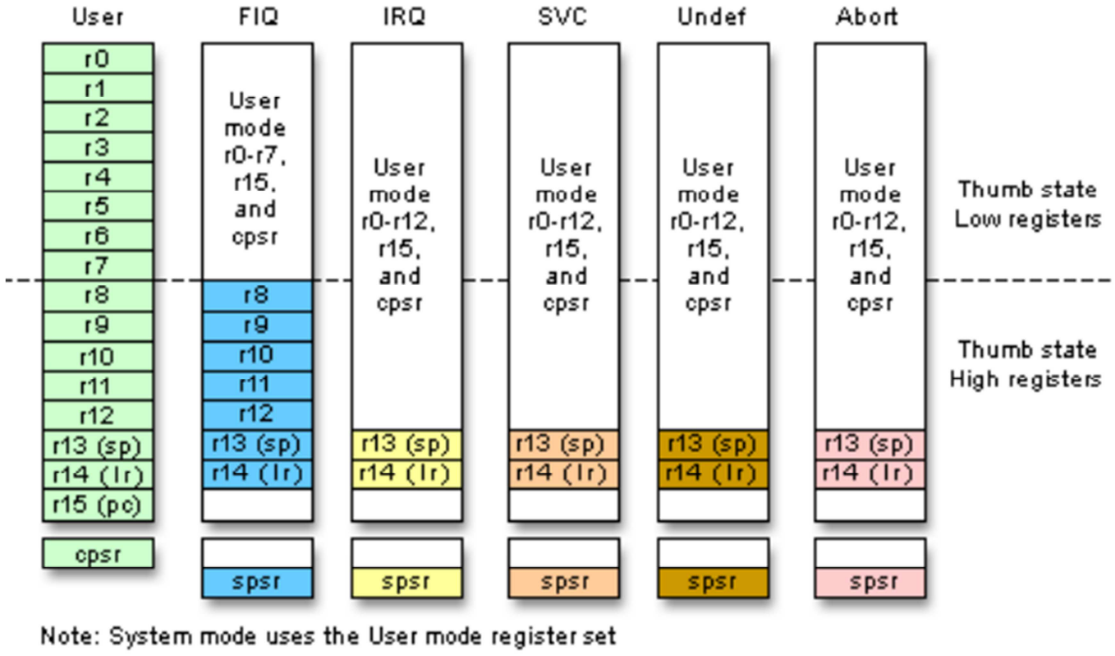

Figure 2. Register organization [5].

Every additional mode provides provide a registers which are use by exception handling routine. These additional registers preserve the state of processor, save location in code and switch between modes. FIQ modes has an additional five

Banked registers. This provide the more flexibility and higher performance when handling critical interrupts.

When ARM core is in Thumb state, the register banks are dividing into low and high register domains. The majority of instructions in Thumb state have a 3 bit register specify. These instructions can access the low registers in Thumb, R0 to R7. The high registers, R8 to R15 are more restricted to use. Only a few instructions can access these registers.

4.2. Data Processing Instructions

The ARM architecture provides the addition, subtraction and bitwise logical operations. This take two 32 bit operands and return a 32 bit result that can be independently specify in 3 address instruction format. The first operand and its result store in the register. Hence, the second operand can be a register or immediate. Next, second operand should be shifted before send to the ALU. There is a limited space for operand specification inside the 32 bit instruction. So, ARM supports the binary comparison operations. This does not return any value but only modify the condition flags in CPSR.

4.3. Data Transfer Instructions

There are two types of data transfer instructions in ARM processor.

1. Single register transfer provides a flexibility to move 1, 2 or 4 byte blocks between registers and memory.
2. Multiple register transfer is very efficient but it is a less flexible. Because, it moves the larger amount of data.

4.4. Control Flow Instructions

ARM architecture provides support for conditional execution of arbitrary instructions. Any instruction can use the value of CPSR condition flags. ARM use a branch and link instruction which save the address of the instruction following the branch to R14. [1]

4.5. ARM Pipeline

Pipeline mechanism increases the execution speed. The pipeline design of each processor family is different.

4.5.1. The 3-Stage Pipeline

The original 3 stage ARM pipeline remain unchanged from the first ARM processor to ARM7TDMI core. This is a classical fetch-decode-execute pipeline. In the absence of pipeline hazards and memory access, it completes in one cycle. The first pipeline stage reads the instruction from memory and increment the value of instruction address register. This store the value of next instruction which is to be fetch, we store this value in PC register. In second stage, decode the instruction and prepare control signals require to execute on it. In the third stage, we reads the operands from register file, perform ALU operations, reads/write memory and if is compulsory write back modified register values.

4.5.2. The 5-Stage Pipeline

The 5-stage ARM pipeline represents the availability of one memory port. It means that each data transfer instruction create a pipeline stall. The next instruction cannot fetch when memory is read/write. There is a one way to remove this problem. We use this in ARM9TDMI and later micro architecture. We separate the instruction and data caches. This avoids the stalls on data transfer instructions.

First, ARM9TDMI move the register read to the decode stage. While, instruction decode stage is shorter than the execution stage. Second, the execute stage divide it into 3 stages. The first stage performs arithmetic computations, second stage performs memory access and the third stage writes the results back to the register file.

This is a balance pipeline, which can run at faster clock. There is a one complication that we need to forward data among pipeline stages to resolve data dependencies.

4.5.3. The 6-Stage Pipeline

In the fetch stage, we fetch two instructions in each cycle, this enable the introduction of a static branch prediction unit. This branch predictor predicts the backward pointing branches as taken and forwarding pointing branches as not taken. This algorithm removes the penalty of branches for loops which execute several times. In the execution stage of pipeline, 64 bit data bus improve the performance of multiple register transfer instructions by transferring two registers at a time.

Next, ARM10 unload the execution stage when it introduces the separate adder for multiply-accumulate instructions instead of using ALU for addition. While, multiply instructions do not read/write. But, adder is place to the data stage, which balances the pipeline and run at a higher clock rate.

Hence, memory access stage becomes the longest running pipeline stage. To remove this problem, we introduce another adder to address computation. This adder computation is a simple addition while this adder can complete its computation in less than a 1 cycle. This effectively leaves one and a half cycles for the memory access. Lastly, the ARM10 is a separation of instruction decoding into a separate stage.

4.5.4. The 8-Stage Pipeline

The ARM core develops two main changes to the pipeline architecture. First, we shift the operation separated into a separate pipeline stage. In second, instruction and data cache access distribute across 2 pipeline stages. 8-stage pipeline divide into three separate pipelines.

5. Memory Hierachy

5.1. Cache

All modern ARMS based processors have on chip L1 cache or on chip memory. Cache divides into separate instruction and data caches. The instruction cache is read only, while data caches are read/write with copy back write strategy.

5.2. Memory Protection

There are two types of memory protection. In first type, simple systems run a predefined set of applications and do not require full feature protection. The protection unit does not provide address translation. This defines eight regions within the 4-gigabyte physical address space; allow access permissions and cache-ability attributes to individual regions.

In second type, fast context switch extension (FCSE) which allows multiple processes to use similar address ranges. FCSE avoid the overhead of removal caches while performing a context switch. So, it is necessary to flush TLBs.

6. ARM ISA Extensions and Cortex Series

6.1. Thumb

Thumb introduced in the fourth version of ARM architecture. This increase the code density for embedded applications. Thumb provides mostly in 32 bit ARM instructions and compress into 16 bit wide op-codes. Thumb code uses 40% more instructions than equivalent 32 bit ARM. This requires 30% less space. Thumb code is 40% slower than ARM code. so, thumb is use only in non performance critical routines in order to reduce memory and power consumption of the system.

6.2. Jazelle

Java virtual machine allows ARM processors to execute java byte code.

6.3. DSP Extensions

ARM based systems perform signal processing tasks. This can use dedicated DSP coprocessors. It is convenient to use DSP support to ARM core. This extension introduce in the fifth version of the architecture. While in the sixth version of ARM architecture, DSP support into SIMD instruction set extension.

6.4. Trust Zone

This extension creates the trusted computer base (TCB) within a SoC. The TCB perform security related tasks, secure software upgrades, etc [2].

There are four types of cortex series cortex-A, cortex-R cortex-M and Secure core.

6.5. Cortex-A Series

Cortex – A is an application processor. These applications are related to the media, graphic, net book, smart book and next generation of digital TV systems. Cortex-A is mostly using in smart phone devices.

Now, we see the performance of Cortex-A series in tabular form.

Table 2. Performance Cortex-A Series.

Cortex-A Series	Performance
Cortex-A 15	Next generation mobile
Cortex-A 12	Mobile, Smart Phone and Tablet devices
Cortex-A 7	Implement in standalone, multi-core
Cortex-A 9	5000 DIMPS performance per core, multi-core
Cortex-A 8	2000DIMPS of performance, Single-core solutions
Cortex-A 5	1200DIMPS of performance, low-cost implement

6.6. Cortex-R Series

Cortex-R Series is a real time embedded processors. These real time applications require less power and good interrupt behaviour. There are many applications like networking & printing, mass storage controller etc.

6.7. Cortex's-M Series

Cortex-M Series is an embedded processor. These processors are developing primarily for the microcontroller domain. There are many applications like microcontrollers, mixed signal device, smart sensors etc.

6.8. Secure Core

Secure core is a specialist processor. These processors are design to meet the needs of specific markets.

ARM also develops processors for FPGA fabrics, enabling users to rapidly reach market while maintaining compatibility with traditional ARM devices. Additionally the fabric independent nature of these processors enables developers to choose the target device which is right for their application rather than be locked to a specific vendor. [9]

7. Smartphone

ARM is the world leading provider of semiconductor intellectual property (IP) for the design of SoC. ARM is at the heart of Smartphone in your pocket today.

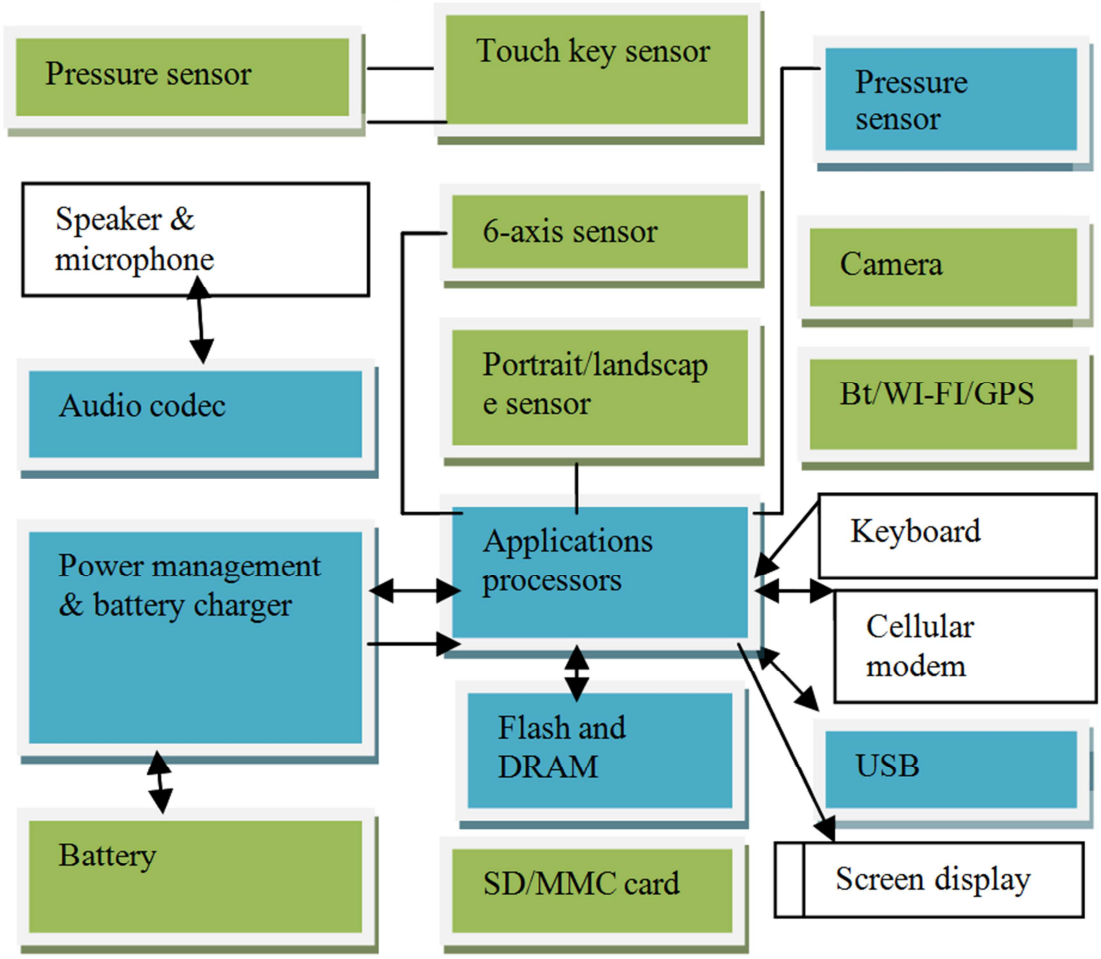

Figure 3. Block Diagram Of Smartphone.

Smartphone components are similar to desktop computer but there is some more components inside the Smartphone. These components are CPU, GPU, other Coprocessors, motherboard buses, memory controller, sound chipset, CMOS camera interface, on-board memory, and several peripheral devices like Wi-Fi, Bluetooth etc. The application processor is the chip which is responsible for general processing and various functions built into it. The baseband processor is responsible for wireless communication.

Smartphone is a consumer device which allows them to manage their online and offline lives. Consumers are using the following tasks:

Access the Internet including social networking sites Face book, YouTube, MySpace and Twitter.

Create and consume multimedia. This include HD video and online content using Adobes Flash Player 10.1

GPS navigation

Gaming includes the latest Open GL ES 2.0 technology.

Messaging from SMS to Email [6]

8. System on a Chip (SoC)

Processor inside a Smartphone device is referring to a system–on-a-chip. SoC is a combination chipset which include the actual processor cores, graphic chipset, RAM, ROM and interface controller such as USB and wireless technology.

SoC cover the small area and reduce the size of component. This also reduces cost of assembling product. Here, we discuss some popular SoCs.

8.1. Qualcomm Processors and Snapdragon SoCs

Qualcomm is different to the other SoC. This does not use the reference ARM core designs. They make their own Scorpion and Krait CPU. They improve their package from ARM Cortex-A8. Qualcomms Snapdragon SoCs divide into different series. Series is numbered from S1 to S4, higher the series the more powerful SoCs. There are no products on the market which use Qualcomm S4 chipsets. S1 and S2 Snapdragon SoCs are single core and it ranges up to 1.5

GHZ. While, S3 Snapdragon is a dual core SoCs and higher graphic as compare to S1 and S2. These devices are using 45 nm processes and Scorpion cores used still Cortex-A8 based. Lets we see important feature of each series.

S1 supports 720p displays, 720p playback and 720p video recording, 12 megapixel and HSPA radio.

S2 improves by adding support for HPSA. Graphics of S2 is better than S1.

S3 supports WSXGA displays, 1080p playback, 1080p recording, stereographic 3D capabilities, dual camera and 16 MP cameras.

Qualcomm SoCs are mostly popular in HTC Smartphone devices.

8.2. Texas Instruments OMAP SoCs

Texas Instruments OMAP (open media application platform) SoCs are also widely used. This is mostly use in the Motorola Smartphone and android devices. The OMAP1 and 2 series are old, we cannot find them in any new Smartphone devices, but OMAP 3 and 4 are use in new Smartphone devices. The TI OMAP 3 series is a single core SoCs which is base on ARM Cortex-A8. The clock speed is 600 MHZ to 1 GHZ and GPU inside is the Power VR SGX530. The TI OMAP 4 series is a dual core SoC which is base on ARM Cortex-A9. The clock speed is 1 GHZ to 1.8 GHZ and GPU inside is the Power VR SGX54x.

TI OMAP series includes the following features:

TI includes smart- reflex power saving technology in the OMAP line. This provides the 10+hours of 1080p playback and 120 hours of audio playback.

TI includes the IV 2/3 multimedia accelerator included on SoC die separate from the Cortex-A8/9 cores. So, this deals with up to 1080p media encoding and decoding on the fly.

OMAP 4 series include two extra ARM Cortex-M 3 cores. This conserves the power and save battery life.

The main disadvantage of TI OMAP series is that wireless radios and several other components are not included inside the chipset as they are in Snapdragon series.

8.3. Samsungs Exynos SoCs

Samsungs Exynos SoC is quite small while, it is middle ground between TI OMAP and Snapdragon SoC. Samsungs Exynos SoC is only inside the Samsung Smartphone and tablets.

The first generation of Samsungs Exynos SoC is a single core feature and base on the Cortex-A8 processor core. The first Samsungs Exynos SoC inside the Samsung Galaxy is known as Samsungs Exynos 3310. The clock speed of this SoC is 1 GHZ while PowerVR SGX540 graphics accelerator is also included. This single core SoC supports full 1080p encode and decode in the original Exynos 3310.

The second generation of Samsungs Exynos SoC is a dual core feature and base on the Cortex-A9 processor core. The Samsungs Exynos 4210 is a very powerful ARM Mali-400 MP4 GPU. The clock speed of this SoC design is 1 GHZ while 1.2 GHZ in Samsung Galaxy SII and 1.4 GHZ in the Galaxy note.

Now, we see some features of Samsung Exynos:

Exynos 4210 improve speed, include GPS capabilities and easier to incorporate different radios into the system.

The Exynos does not support 3D displays, recording and decoding. There is no media accelerator, so it must be decoded either on GPU or CPU. It does not affect performance of Galaxy Note because it supports huge range of codes that play fine.

Exynos 4210 display resolution 1280 x 800 (WXGA) vs. Snapdragon S'3 1440 x 900 (WSXGA) and TI OMAP 4'S 1920 x 1200 (WUXGA). While, its output is 1080p over HDMI, but it cannot support 1080p interface display.

8.4. NVIDIA's Tegra SoCs

This SoC is design for graphics purposes and we enhance the GPU department. There are two types of Tegra SoC, Tegra 2 and Tegra 3. This is widely use in the Smartphone and Tablets devices. Both are multi-core and base on ARM-Cortex-A9 cores in the SoCs. The clock speed is range from 1 to 1.4 GHZ, while both are using a 40nm process and ultra low power (ULP) GeForce GPU as the graphic chip.

8.5. Apple SoCs

Apple SoC is a last series of a SoC. These SoCs are not licences while other SoCs are licence. These SoCs are use inside the Apple products such as iPhone, iPad, iPod and Apple TV. Now a day's Apple using the Apple 4 and Apple 5 in the iPad and iPhone.

A4 is a single core which includes a single ARM Cortex-A8 core. The clock speed is 800 MHZ-1.00 GHZ and a PowerVR SGX535 GPU. This made 45 nm processes and includes ARM's MPE which allows NEON code.

A5 is a dual core ARM Cortex-A9 CPU and a dual core PowerVR SGX543MP2 GPU. Main features are same to A4 like MPE, clock speed and 45 nm processes. There is a 512 RAM and image signal processor (ISP) in the A5.

Now, we will see the most of the major Smartphone processors families in the market today. Here is a table which describe the whole overview of Smartphone processors.

9. Which Is Best

It is very hard to say that which SoC is best.

The performances of ARM –Cortex series remain same in the Smartphone devices while the graphics chip makes the huge difference to the overall performance.

The non-graphic performance can be improve from other components. These components are included in the SoC separately from the actual cores. For example, Tegra 2 chips lack the ARM Advance SIMD.

The lot of SoC manufactures find the interesting way to save the power in the chipset. for example, Tegra 3 and TI OMAP 4 series. Here is a important that, SoC is not responsible for battery life.

In terms of actual size, the Snapdragon advantage to manage the processing cores, graphic chip, media accelerator, wireless radios, GPS and RAM. This save the data on other chips while PCB can be cut down. This provide space for batteries, so our device becomes very slim.

There are other components which are not fully use in the device. For example, 16 MP of camera display resolutions up to 1920 x 1200 with 1080p.

So, we cannot answer this question. It depends upon the user requirement which he select for video player, HD, games, graphics features etc. [7]

9.1. ARM vs. Intel

Intel designs and builds their own processors while ARM creates the instruction sets. ARM allows many companies to produce their own chipsets around ARM s core designs. Intel's failure due to completely missing the Smartphone and tablet revolution, which started with Apple's i-Phone in 2007.

Intel didn't complete the market demand for lower power chips which prolonged battery life on these devices.

But Intel compete the whole array of ARM licensees in the coming years. [10]

9.2. Future of ARM Processor for Smartphone Devices

ARM cortex series is very popular series in Smartphone devices. So, in the future new cortex series will use in smart phone devices use 64-bit support in the ARM processor architecture. Its main focus on power efficient implementation and maintain the existing 32-bit software. ARM v8 processors will be use such as cortex-57 and cortex-53. This enhances the performance range and consumes the low power. This benefit is use in Smartphone devices which handle the applications such as video and servers processing in web transactions. These processors use 64-bit support and new range of hardware capabilities. These new processors support virtualization, error correction, security and floating point. [11]

9.3. Smartphone Overview

Now, we will see the most of the major Smartphone processors families in the market today. Here is a table which describe the whole overview of Smartphone processors.

Table 3. Overview of Smartphone Processors.

Mobile Chipset	Application Processor	Instruction on Set	Integrated/Paired 3D graphics	Clock Speed	Phone Examples
Qualcomm MSM72xx	ARM1136J-S	ARMV6	None /ATI	523 MHZ	HTC
Marvell XScale PXA320	Marvell XScale	ARMV5	None	800 MHZ	Samsung Omni
Samsung S3C6xxx	ARM1136JF-S	ARMV6	None/Power SGX-Lite	800 MHZ	Apple iPhone, Samsung Omina II
Samsung S5PC100	ARM Cortex A8	ARMV7	PowerVR SGX 535	833MHZ	Apple iPhone 3GS
TI OMAP3	ARM Cortex A8	Armv7	PowerVR SGX 530	500 MHZ	Palm pre
Qualcomm QSD8250	Qualcomm Scorpion	ARMV7	ATI Imageon Z430	1.000 MHZ	HTC HD2.
Nvidia Tegra APX2500	ARM11 MPCore	ARMV6	Nvidia Tegra	600 MHZ	None yet
Nvidia Tegra 250	Dual core ARM Cortex A9	ARMV7	Nvidia Tegra		None
Reference Intel Atom N270	Intel Atom	X86	Intel GMA950	800 MHZ-2 GHZ	None

10. Conclusion

ARM is a 32 bit RISC processor. ARM processor is designed and licensed by British company ARM holding. In 2010, ARM processors reported the shipments of 6.1 billion, represents the 95% of smart phone, 35% of digital televisions and 10% of mobile computers. Design of ARM processor is very simple and covers very less space as compare to powerful RISC machine. ARM's goal is to optimize the price and performance ratio rather than building the most powerful processor in the market. ARM lies at the heart of digital products, mobile phone, digital camera and automotive system.

ARM is a leading intellectual property (IP) of high performance, low cost, power efficient and system on chip (SOC) designs with the different organizations. ARM architecture is compatible with all major operating systems

such as Symbian OS, Palm OS, LINUX and Windows CE.

ARM also provides the software solutions to existing market segments. ARM are at the heart of Smartphone in your pocket today.

Now a day, ARM Cortex series is very popular in Smartphone devices. SoC is a combination chipset which include the actual processor cores, graphic chipset, RAM, ROM and interface controller such as USB and wireless technology. Now a day, Snapdragon, Nvidia Tegra, Texas instruments OMAP, Apple and Samsung Exynos. It is very hard to say that which SoC is best. Each SoC has its own properties. It depends upon the user requirement which he select for video player, HD, games, graphics features etc.

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