Physics Journal
Vol. 2, No. 1, 2016, pp. 11-14
http://www.aiscience.org/journal/pj

AIS American Institute of Science

Influences of Channel Width and Oxide Thickness on the Threshold Voltage of Fully-Depleted Four-Gates Field Effect Transistor

M. Salami, M. H. Shahrokh Abadi*

Faculty of Electrical and Computer Engineering, Hakim Sabzevari University, Sabzevar, Iran

Abstract

A mathematical model of fully-depleted ultrathin silicon on insulator with buried oxide and four individual gates field effect transistor (G4-FDSOI-FET) has been developed to determine the effects of the oxide thickness as well as the channel width on the threshold voltage. Two dimensional Poisson's equation has been carried out to model the device. The results show that the threshold voltage depends on the back surface conditions and is a function of structural parameters of oxide thicknesses of front and back gates as well as the width and thickness of the channel.

Keywords

Fully Depleted, Multi-Gate, Threshold Voltage, Silicon on Insulator, MOSFET

Received: September 14, 2015 / Accepted: October 14, 2015 / Published online: December 6, 2015

@ 2016 The Authors. Published by American Institute of Science. This Open Access article is under the CC BY-NC license.
http://creativecommons.org/licenses/by-nc/4.0/

1. Introduction

Multiple-gates silicon-on-insulator metal-oxide-semiconductor transistors (Mu-SOI-MOS) have been developed from classical, planar, and single gate devices into three dimensional devices. SOI devices are popular for very low parasitic capacitance, better radiation tolerance and better isolation in both horizontal and vertical direction. Studies shown that the planar fully depleted (FD) SOI MOSFETs can be suitable candidates for the continually scaling CMOS [1-4] due to their capabilities to reduce the subthreshold slope [5], minimize the short-channel effects (SCEs) [6], and increase the transconductance [7].

Recent studies have shown that the increasing the number of gates can reduce the SCEs, therefore multi-gate structures are desired. Among the multi-gate FETs (MuG-FETs), the four-gate field effect transistors (G^4-FETs) on an insulator, have the unique capability of utilizing four independent gates to modulate the current in the channel [8-12]. Furthermore, with increasing the number of gates, the number of transistors in the circuit will be reduced in contrast with the conventional CMOS implementations.

Since SOI films are thin, the electrical properties of MOSFET's, e.g. the threshold voltage (V_{TH}), are typically influenced by the charge coupling between gates. In this paper, an analytical model of threshold voltage in an FDSOI-G^4-FET with respect to different back-surface charge conditions is investigated and the influences of different oxide as well as the channel thicknesses on the threshold voltage are studied.

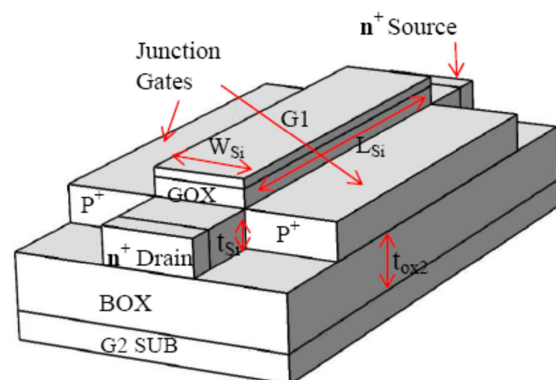

Fig. 1. The structural model of the FDSOI G^4-FET.

* Corresponding author
E-mail address: mhshahrokh@ieee.org (M. H. S. Abadi)

2. Device Structure

The G^4-FET has two (top and bottom) MOS-gates and two (lateral) JFET-gates in which it operates normally in accumulation mode. The end contacts play the role of source and drain in the G^4FET and the side junctions are used as lateral gates. The two MOS-gates are developed on the gate-oxide (GOX) on the top and beneath the buried-oxide (BOX) on the bottom. The current in the body of the device is controlled by these four gates and flowed in the direction perpendicular to that of the p-MOSFET current. The height and width of the conductive path is modulated by combination of the both MOS and JFET effects. When the body is fully depleted, its potential distribution becomes a function of the bias on the four gates. The structure of the G^4FET has been given in Figure 1. Table 1 shows the parameters of the device that have been used during this study.

Table 1. The parameters of G^4-FET.

Channel Doping (N_D)	Silicon Film Thickness (t_{si})	Front and Back Oxide Thicknesses (t_{ox1}/t_{ox2})	Silicon Film Width (W_{si})	Silicon Film Length (L)
1.5×10^{17} cm^{-3}	50 nm	12/400 nm	500 nm	3 µm

3. Analytical Mode

For the analytical modeling purpose, the device has been considered as an n-channel thin film FD-G^4-FET. Front-gate (V_{G1}), back-gate (V_{G2}) and junction-gates ($V_{JG1,2} = V_{JG}$) voltages were chosen so that the channel becomes fully depleted. Using a 2D model of potential distribution, the relation between the maximum surface potential of front and back gates with respect to the applied voltages can be given by [8, 10]:

$$V_{G1} \quad V_{FB1} \quad (1 \quad \frac{C_{jg}}{C_{ox1}}) \quad {}_{s1} \quad \frac{C_{jg}}{C_{ox1}} \quad {}_{s2} \quad (\quad) \frac{C_{jg}}{C_{ox1}} (V_{JG} \quad V_P) \tag{1}$$

$$V_{G2} \quad V_{FB2} \quad (1 \quad \frac{C_{jg}}{C_{ox2}}) \quad {}_{s2} \quad \frac{C_{jg}}{C_{ox2}} \quad {}_{s1} \quad (\quad) \frac{C_{jg}}{C_{ox2}} (V_{JG} \quad V_P) \tag{2}$$

$$\alpha \equiv \frac{2\sqrt{2}}{\tanh(\frac{2\sqrt{2}}{W} t_{si})} \tag{3}$$

$$\gamma \equiv \frac{2\sqrt{2}}{\sinh(\frac{2\sqrt{2}}{W} t_{si})} \tag{4}$$

$$V_P = \phi_B - (qN_D W^2 / 8\varepsilon_{si}) \tag{5}$$

$$C_{ox1} = \varepsilon_{ox} / t_{ox1} \tag{6}$$

$$C_{ox2} = \varepsilon_{ox} / t_{ox2} \tag{7}$$

$$C_{jg} = \varepsilon_{si} / W \tag{8}$$

The variables used in the above equations are described in Table 2.

Table 2. The definition of the variables.

Maximum front and back surface potential	Pinchoff voltage	Potential barrier between the body and the junction gates	Flat-band voltages	Front and back gate oxide capacitance	Lateral depletion capacitance
Ψ_1, Ψ_2	V_p	Φ_B	V_{FB1}, V_{FB2}	C_{ox1},C_{ox2}	C_{jg}

During the operation, accumulation of electrons occurs at the front surface when $\Psi_1 > 0$, so that at the onset of accumulation the maximum surface potential, Ψ_1, becomes zero. For the fully depleted channel, the front-gate threshold voltage is a strong function of back surface condition, so it should be considered individually for various back surface charge conditions.

3.1. Accumulated Back Surface

When the back surface is accumulated, $\Psi_2 = 0$, therefore from Eq. 1, the threshold voltage can be stated as:

$$V_{T,G1}^{G2,acc} = V_{FB1} + (\gamma - \alpha) \frac{C_{jg}}{C_{ox1}} (V_{JG} - V_P) \tag{9}$$

This mode of operation is not practical because the back-channel current acts as leakage current and shunts the G[4]-FET.

3.2. Inverted Back Surface

Since the quasi Fermi levels are separated by V_{JG}, the back potential required to achieve the inversion is given by $\Psi_2 = V_{JG} + 2\Phi_F$, where $\Phi_F = -V_t \ln(N_D/n_i)$ is the difference between the extrinsic and intrinsic Fermi levels for n-type channel. Applying these criteria in Eq. 1 yields:

$$V_{T,G1}^{G2,inv} = V_{FB1} - \gamma \frac{C_{jg}}{C_{ox1}}(V_{JG} + 2\phi_F) + (\gamma - \alpha)\frac{C_{jg}}{C_{ox1}}(V_{JG} - V_P) \quad (10)$$

3.3. Depleted Back Surface

In this mode, Ψ_{s2} can be obtained by the following equation:

$$\psi_{s2} = \frac{V_{G2} - V_{FB2} + (\gamma - \alpha)\frac{C_{jg}}{C_{ox2}}(V_{JG} - V_P)}{(1 + \alpha \frac{C_{jg}}{C_{ox2}})} \quad (11)$$

Substituting Eq. 11 into Eq. 1 and setting $\Psi_1 = 0$, threshold voltage can be found as:

$$V_{T,G1}^{G2,dep} = V_{FB1} - \beta(V_{G2} - V_{FB2}) + (\gamma - \alpha)(\frac{C_{jg}}{C_{ox1}} + \beta\frac{C_{jg}}{C_{ox2}})(V_{JG} - V_P) \quad (12)$$

where

$$\beta = (\gamma \frac{C_{jg}}{C_{ox1}}) / (1 + \alpha \frac{C_{jg}}{C_{ox2}}) \quad (13)$$

4. Results and Discussion

4.1. Impact of Front and Back Gate Oxide Thickness

Using Eq. 6 and Eq. 8 and at $V_{JG} = 0$ V, the threshold voltage of the device for different values of structural parameters has been calculated and shown in Figures 2 and 3 for depletion and inversion modes, respectively. Figure 2 shows the variations of threshold voltage versus front and back gate oxide thickness. As it can be seen from Figure 2(a), the threshold voltage is a linear function of front gate oxide thickness (t_{ox1}) and for both depleted and inverted back surface it is increased when the t_{ox1} is increased. This is due to the reducing of the field strength at a fixed gate voltage for a thicker oxide.

It is also clear from Figure 2(b) that when the back surface is inverted, the threshold voltage remains constant with changing the oxide thickness, shows an independency to the oxide thickness. When the back surface is depleted and the back oxide thickness is varied between 5 nm to 60 nm, the magnitude of the voltage is slowly increased with increasing t_{ox2}. Furthermore, in comparison between the inverted back surface and the depleted, the magnitude of the threshold voltage shows higher value for the inverted back surface at the same position.

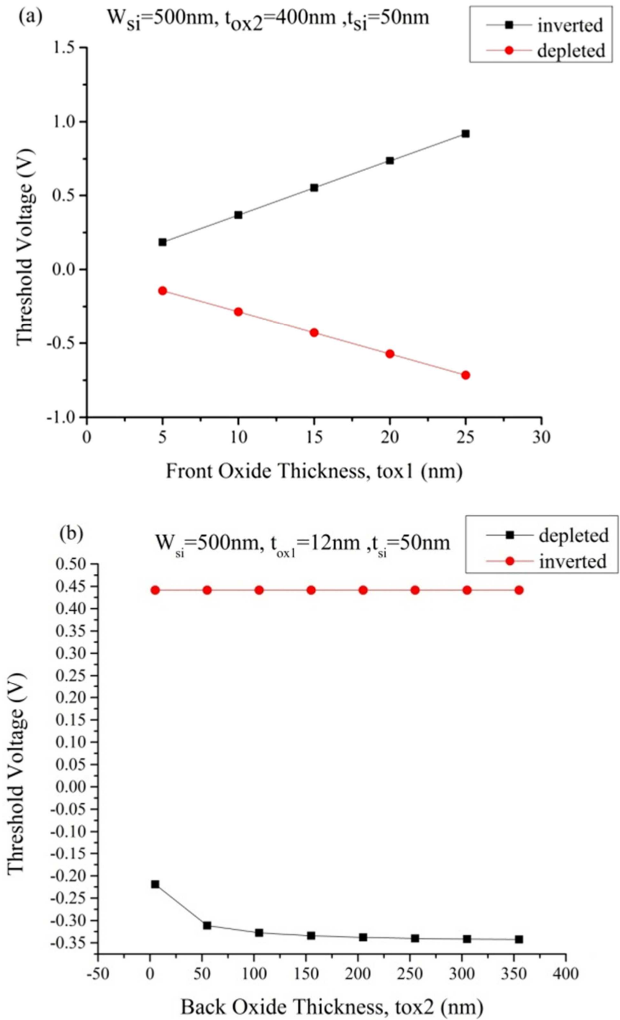

Fig. 2. Threshold voltage of G[4]-FET as a function of (a) front oxide thickness, (b) back oxide thickness for depleted and inverted back surface.

4.2. Impact of Silicon Film Thickness and Width

Figure 3(a) shows that the threshold voltage is a nonlinear function of the silicon film width. From this figure, it can be observed that the magnitude of the voltage decreases with increasing silicon film width (W_{si}) for the both inverted and depleted back surface, respectively. This can be interpreted as the degrading of the lateral depletion capacitance related to the junction gates.

When the back surface is inverted (Fig. 3(b)), a reduction in

the silicon film thickness (t_{si}) causes an increment in the magnitude of the threshold voltage. This is because while the film thickness is decreased, the natural length of the device degrades and both the concentration of inversion carriers and the minimum energy of the sub-bands are increased. Furthermore, when the back surface is depleted, decreasing the film thickness leads to reduction of the threshold voltage.

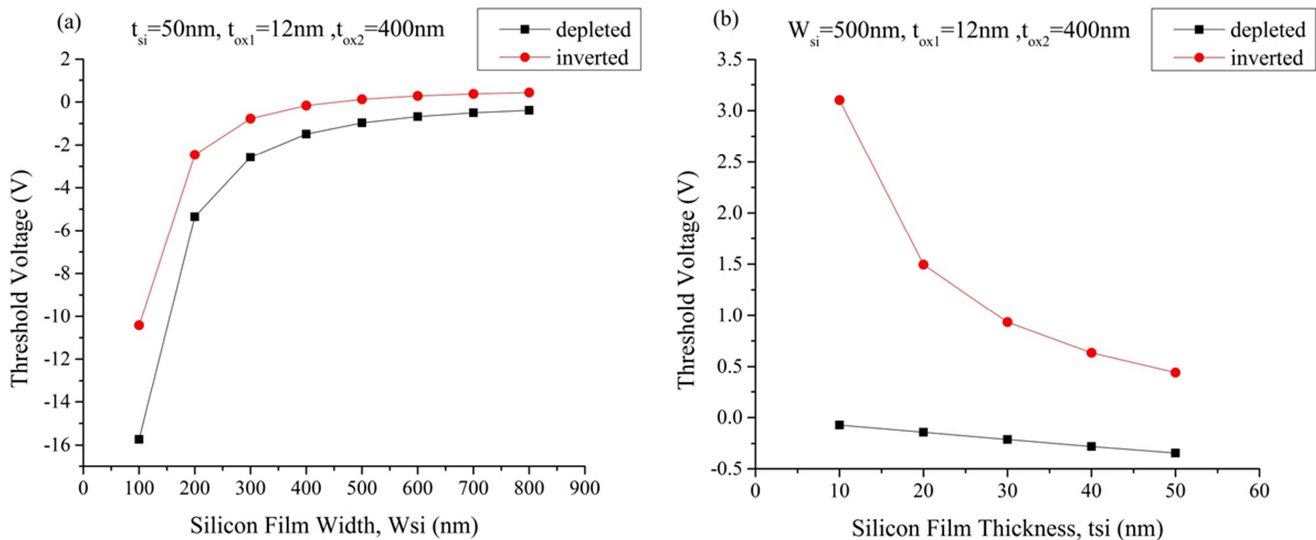

Fig. 3. Threshold voltage of G4-FET as a function of (a) Silicon film thickness and (b) Silicon film width for depleted and inverted back surface.

5. Conclusion

The results show that the threshold voltage of the G4-FET can be controlled by varying the structural parameters of front and back oxide thickness as well as width and thickness of channel. For thinner front and back oxide gate, the magnitude of the threshold voltage is lowered when the back surface is depleted or inverted. For the inverted back surface, with decreasing of width and thickness of silicon film, the magnitude of the threshold voltage is strongly increased. For the depleted back surface, with decreasing the width of silicon film, the magnitude of the voltage is increased and vise verse.

References

[1] Rahou FZ, Bouazza AG, Rahou M. Electrical Characteristics Comparison Between Fully-Depleted SOI MOSFET and Partially-Depleted SOI MOSFET using Silvaco Software. Global Journal of Researches in Electrical and Electronics Engineering. 2013; 13: 1–6.

[2] Fossum JG, Trivedi VP. Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs: Cambridge University Press; 2013.

[3] Mazurier J, Weber O, Andrieu F, Toffoli F, Rozeau O. On the Variability in Planar FDSOI Technology: From MOSFETs to SRAM Cells. Electron Devices IEEE Transactions on. 2011; 58: 2326–2336.

[4] Kumar, Tiwari PK. A Threshold Voltage Model of Short-Channel Fully-Depleted Recessed-Source/Drain (Re-S/D) UTB SOI MOSFETs Including Substrate Induced Surface Potential Effects. Solid-State Electronics. 2014; 95: 52–60.

[5] Vitale SA, Wyatt PW, Checka N, Kedzierski J, Keast CL. FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics. Proceedings of the IEEE. 2010; 98: 333–342.

[6] Ranka D, Rana AK, Yadav RK, Giri D. Performance Analysis of FD-SOI MOSFET with Different Gate Spacer Dielectric. International Journal of Computer Applications. 2011; 18: 22–27.

[7] Fernandez C, Rodriguez N, Ohata A, Gamiz F. Bias-Engineered Mobility in Advanced FD-SOI MOSFETs. IEEE Electron Device Letters. 2013; 34: 840–842.

[8] Sayed S, Hossain MI, Khan MZR. A Subthreshold Swing Model for Thin-Film Fully Depleted SOI Four-Gate Transistors. IEEE Transaction on Electron Devices. 2012; 59: 854–857.

[9] Noor SL, Haq AFMS, Hassan M. Study of Threshold Voltage of p-channel Four Gate Transistor. Informatics, Electronics & Vision (ICIEV), IEEE International Conference on. 2013; 1–4.

[10] Akarvardar K, Cristoloveanu S, Gentil P. Analytical Modeling of the Two-Dimensional Potential Distribution and Threshold Voltage of the SOI Four-Gate Transistor. IEEE Transactions on Electron Devices. 2006; 53: 2569–2577.

[11] Sayed S, Hossain MI, Huq R, Khan MZR. Three Dimensional Modeling of SOI Four Gate Transistors. IEEE Nanotechnology Materials and Devices Conference. 2010; 383–388.

[12] Sayed S, Khan MZR. Analytical Modeling of Surface Accumulation Behavior of Fully Depleted SOI Four Gate Transistors (G4-FETs). Solid-State Electronics. 2013; 81: 105–112.