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Analytical Investigation of Triple-Material Cylindrical Gate-Surrounded (TM-CGS) MOSFETs with High-K Material Oxide

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Abstract

An analytical model for the short channel cylindrical / surrounding gate MOSFET based on the solution of Poisson's Equation in the parabolic approximation of the potential along the radial axis is presented in this work. Three different electrodes, having different work-functions, and three different high-k dielectric materials have been used as thegate contacts and the gate oxides, respectively, to prevent direct tunneling leakage current in the device. The center and the surface potential models have been obtained by solving the 2-D Poisson's equation in the cylindrical coordinate system. The effects of physical parameters such as cylinder diameter, oxide thickness, gate length ratio, natural length of the center potential, and sub-threshold swing have been investigated in the device by using MATLAB simulator. The results show that introducing triple high-k material can modify the impact of drain-induced barrier lowering, DIBL. A significant decrease in the center potential due to applying different gate oxides has been observed and compared to those with single oxide film.For further verification of the results, a calibrationapproach for the device performance has been also taken into account.

Keywords

MOSFET, Gate Surrounded, Poisson's Equation, Short Channel Effect, Drain Induced Barrier Lowering, Subthreshold Swing

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1. Introduction

As conventional MOSFETs are scaled down to several nanometers, short channel effects (SCEs) such as the threshold voltage roll off due to charge sharing between drain/source and channel, Drain Induced Barrier Lowering (DIBL) due to the variation of the source/channel barrier by the drain voltage and hence an increase in the off state leakage current, punch throughdue to merging the depletion layers around the drain and source regions into a single depletion region, etc are happened. Therefore, reducing short channel effects plays major role in scaling the MOS devices [1, 2]. Gate engineering with having more than one gate over the channelincluding: Double Gate, Pi Gate, Triple Gate, Finger-Shaped Gate, Omega Gate, and Surrounded/Cylindrical Gateare some of the solutions to overcome the effects. The improvement in the device performance, however, is believed to be continued in association with multigate MOSFETs as they employ third dimension, offering superb gate control over the channel from several sides [3]. Among the various multigate structures, triple-gate MOSFET makes the channel engaged from three sides giving improved on-state current and reduced off-state current, and between these structures, cylindrical/surrounded (CGT/SGT) gate MOSFET offers higher packing density, steep subthreshold characteristics and higher current drive [4, 5]. Another superior feature of this structure is that the gate surrounds the silicon pillar completely and hence controls the channel potential in a more effective manner causes to increase short channel immunity,compared to the single and double gate structures [2, 6]. Another issue of short channelcan occur with

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reduction of gate dielectrictickness. The effect brings aboutthe direct tunneling leakage current that raises static power consumption and can disturb the device operation. The use of high-k gate oxide keeps the right equivalent oxide thickness (EOT) and elevates the gate capacitance with low leakage current, resulted in higher on-state current [7, 8]. Although the short channel performance decrease with the increace in the gate dielectric constant due to increased fringing field either from the gate to the source/drain regions or from the source/drain to the channel region which weakens the gate control, to overcome the limitation, high-k dielectrics along with $SiO_2$are used [7-11]. For a moderately doped MOSFET, the center of the channel is inverted more than the channel surface, and hence classical model for the threshold voltage may not be valid [3], [12-14].

In thecurrent work, combination of a high-k material over the silicon oxide,on triple material CG MOSFET [15] has been investigated andresolved the channel potential at the center of cylindrical instead of the surfaceby using 2-D analytical model to observe the impact of the structure on device characteristic such as the natural lengths, sub-threshold swing and DIBL.

2. Device Modeling

The schematic of the TM-CGS MOSFET used for the center potential and sub- threshold voltage modeling is shown in the Fig. 1, where the notations L, t_{si}, t_1, t_2 are the channel length, silicon film thickness, gate-oxide thickness and high-k dielectric thickness of the device, respectively. N_A is doping concentration in the silicon. φ_1 , φ_2 and φ_3 , the work-functions of gate materials,are Au = 4.8eV, Mo = 4.6eV and Ti = 4.4eV, from source to drain, respectively.

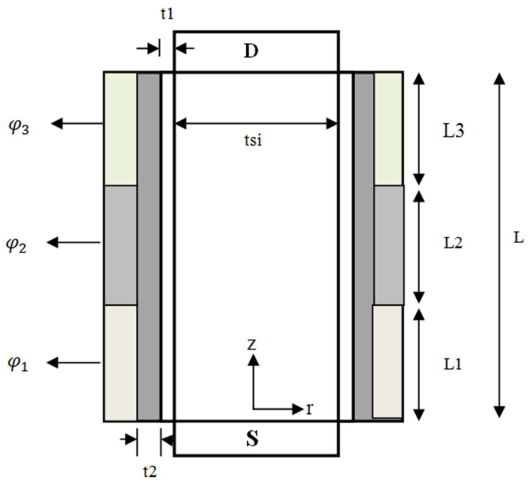

Fig. 1. Schematic diagram of TM-CGS MOSFET. Channel length, L=30 nm, p type substrate doping $N_A = 1 \times 10^{16}$ cm^{-3}, moderately doped source/drain, $N_D = 1 \times 10^{20}$ cm^{-3}, silicon channel thickness tsi, SiO_2 thickness t_1, High-k dielectric thickness t_2,dielectric permittivity of SiO_2 and high K dielectric ε_1 and ε_2 respectively.

2-D Poisson's equation for potential, $\emptyset(r,z)$, in cylindrical coordinates is defined as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\emptyset_i(r,z)\right)+\frac{\partial^2}{\partial z^2}\emptyset_i(r,z)=\frac{qN_a}{\epsilon_{si}} \quad (1)$$

where The subscript i = 1, 2, and 3 are used for channel regions I, II, and III, respectively, N_a is the channel doping, q is the electronic charge and ϵ_{si} is the permittivity of the Si film.

A parabolic solution in the radial direction is assumed as:

$$\emptyset_i(r,z)=C_{0i}(z)+C_{1i}(z)r+C_{2i}(z)r^2 \quad (2)$$

where the coefficients can be found from the boundary conditions as they follow:

1) The potentials at the body center $\emptyset_{ci}(z)$ and at the surface $\emptyset_{si}(z)$ are, respectively, given by:

$$\emptyset_i(0,z)=\emptyset_{ci}(z)=C_{0i}(z) \quad (3)$$

$$\emptyset_i\left(\pm\frac{t_{si}}{2},z\right)=\emptyset_{si}(z) \quad (4)$$

2) The electric field in the center of the silicon pillar is zero by symmetry.

$$\frac{d}{dr}\emptyset_i(r,z)=C_{1i}(z)=0 \quad (5)$$

3) The electric field at the silicon/oxide interface can be derived from the gate potential, $\emptyset_{gsi}=Vgs-V_{fbi}$, (that $V_{fbi}$are the channel flat-band voltages of Si film given by $V_{fbi}=\varphi_{Mi}-\emptyset_w$, and φ_{Mi} represents the metal work functions above the regions I, II, and III, and $\emptyset_w$ is silicon work function) the surface potential ($\emptyset_s$), and silicon pillar and gate oxide thicknesses

$$\frac{d}{dr}\emptyset_i(r,z)\Big|r=\frac{t_{si}}{2}=\frac{\epsilon_{ox}}{\epsilon_{si}}\left(\frac{\emptyset_{gsi}-\emptyset_{si}(z)}{\frac{t_{si}}{2}\ln(1+\frac{2t_{eff}}{t_{si}})}\right)=t_{si}C_{2i}(z) \quad (6)$$

$$t_{eff}=t_1+\frac{\epsilon_1}{\epsilon_2}t_2 \quad (7)$$

t_{eff} is the effective silicon oxide thickness t_1 is the thickness of the SiO2 (ϵ_1) layer and t_2 is the thickness of the high-k layer (ϵ_2).

4) Potentials at source–channel and drain–channel interfaces are, respectively, given by:

$$\emptyset_1(r,0)=V_{bi} \quad (8)$$

$$\emptyset_3(r,L_1+L_2+L_3)=V_{bi}+V_{DS} \quad (9)$$

Where V_{bi} is the built-in voltage between the source/drain and Si channel junction.

5) The potentials and electric fields at the interface of two adjacent gates, respectively, is [3]:

$$\emptyset_1(r, L_1) = \emptyset_2(r, L_1) \quad (10)$$

$$\emptyset_2(r, L_1 + L_2) = \emptyset_3(r, L_1 + L_2) \quad (11)$$

$$\left[\frac{\partial \emptyset_1(r,z)}{\partial z}\right]_{z=L_1} = \left[\frac{\partial \emptyset_2(r,z)}{\partial z}\right]_{z=L_1} \quad (12)$$

$$\left[\frac{\partial \emptyset_2(r,z)}{\partial z}\right]_{z=L_1+L_2} = \left[\frac{\partial \emptyset_3(r,z)}{\partial z}\right]_{z=L_1+L_2} \quad (13)$$

By utilizing (3)–(6) in (2), the center potential and the surface potential can be related as

$$\emptyset_{si}(z) = \emptyset_{ci}(z) + \rho\left(\emptyset_{gsi} - \emptyset_{si}(z)\right) \quad (14)$$

$$\rho = \frac{\epsilon_{ox}}{2\epsilon_{si}\ln(1+\frac{2t_{eff}}{t_{si}})} \quad (15)$$

The resulting solution for $\emptyset_i(r,z)$ after eliminating $\emptyset_{si}$ and Substituting into Poisson's equation (1), We get:

$$\frac{\partial^2 \emptyset_{ci}(z)}{\partial z^2} - \frac{1}{{\lambda_c}^2}\emptyset_{ci}(z) = \beta_i \quad (16)$$

where

$$\beta_i = \frac{qN_a}{\epsilon_{si}} - \frac{1}{{\lambda_c}^2}\emptyset_{gsi} \quad (17)$$

And

$$\lambda_c = \sqrt{\frac{2\epsilon_{si}{t_{si}}^2 \ln\left(1+\frac{2t_{eff}}{t_{si}}\right)+\epsilon_{ox}{t_{si}}^2}{16\epsilon_{ox}}} \quad (18)$$

Where λ_c is natural length.

Solving (18) for three regions I, II, and III, we obtain the center potentials as follow:

$$\emptyset_{c1}(z) = Ae^{\frac{z}{\lambda_c}} + Be^{\frac{-z}{\lambda_c}} - {\lambda_c}^2\beta_1, 0 < z < L_1 \quad (19)$$

$$\emptyset_{c2}(z) = Ce^{\frac{z}{\lambda_c}} + De^{\frac{-z}{\lambda_c}} - {\lambda_c}^2\beta_2, L_1 < z < L_1 + L_2 \quad (20)$$

$$\emptyset_{c3}(z) = Ee^{\frac{z}{\lambda_c}} + Fe^{\frac{-z}{\lambda_c}} - {\lambda_c}^2\beta_3, L_1 + L_2 < z < L_1 + L_2 + L_3 = L \quad (21)$$

By utilizing boundary conditions (8), (9), (10), (11), (12) and (13), we can achieve A, B, C, D, E and F constants as follow:

$$A = \frac{1}{2\sinh(\frac{L}{\lambda_c})}\left[((\lambda_c{}^2\beta_1 - \lambda_c{}^2\beta_2)\cosh(\frac{L_2+L_3}{\lambda_c})) + ((\lambda_c{}^2\beta_2 - \lambda_c{}^2\beta_3)\cosh(\frac{L_3}{\lambda_c})) + (V_{bi} + V_{DS} + \lambda_c{}^2\beta_3) - (V_{bi} + \lambda_c{}^2\beta_1)e^{\frac{-L}{\lambda_c}}\right] \quad (22)$$

$$B = V_{bi} + \lambda_c{}^2\beta_1 - A \quad (23)$$

$$C = A - \frac{(\lambda_c{}^2\beta_1 - \lambda_c{}^2\beta_2)}{2}e^{\frac{-L_1}{\lambda_c}} \quad (24)$$

$$D = B - \frac{(\lambda_c{}^2\beta_1 - \lambda_c{}^2\beta_2)}{2}e^{\frac{L_1}{\lambda_c}} \quad (25)$$

$$E = C - \frac{(\lambda_c{}^2\beta_2 - \lambda_c{}^2\beta_3)}{2}e^{\frac{-(L_1+L_2)}{\lambda_c}} \quad (26)$$

$$F = B - \frac{(\lambda_c{}^2\beta_1 - \lambda_c{}^2\beta_2)}{2}e^{\frac{L_1}{\lambda_c}} - \frac{(\lambda_c{}^2\beta_2 - \lambda_c{}^2\beta_3)}{2}e^{\frac{(L_1+L_2)}{\lambda_c}} \quad (27)$$

Minimum surface potential $\emptyset_{smin}(z)$ of the silicon cylinder will be under the gate having the highest work function (in this case, $\emptyset_{s1}(z)$). The position at minimum of surface potential, Zmin is obtained by $\frac{d\emptyset_{s1}(z)}{z} = 0$.

$$\emptyset_{smin} = 2\sqrt{AB} - (\lambda_c{}^2\beta_1) \quad (28)$$

And the minimum potential occurs at:

$$Zmin = \frac{\lambda_c}{2}\ln\left(\frac{B}{A}\right) \quad (29)$$

The electric field at the SiO_2 / Si junction may be found as [3]

$$E_i = \frac{d\emptyset_{si}(z)}{dz}, i = 1,2 \text{ and } 3 \quad (30)$$

An important parameter characteristic of subthreshold region of MOSFET is subthreshold swing (SS). The subthreshold swing primarily depends on the carrier concentration [2] and is defined

$$SS = \frac{KT}{q}\ln(10)\frac{1}{\frac{d\emptyset_{S1}(z_{min})}{dVgs}} \quad (31)$$

By utilizing of (16), we can achieve:

$$SS = \frac{KT}{q}\ln(10)\left(\left(\frac{1}{\sqrt{AB}}\right)\left[\left(\frac{1}{2\sinh\left(\frac{L}{\lambda_c}\right)}\right)\left(e^{\frac{-L}{\lambda_c}} - 1\right)B + A\left(-1 - \left(\frac{1}{2\sinh\left(\frac{L}{\lambda_c}\right)}\right)\left(e^{\frac{-L}{\lambda_c}} - 1\right)\right)\right] + 1\right)^{-1} \quad (32)$$

3. Model Verification and Calibration

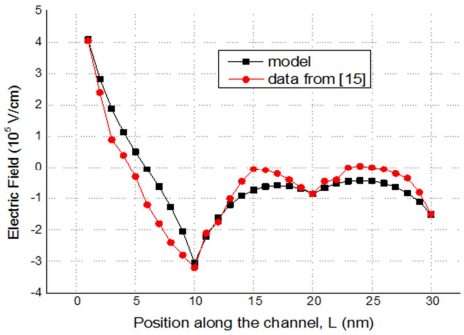

Fig. 2. Comparison between the Electric Field and position along the channel and calibration with published result [15], using: $\varphi_{m1} = 4.8eV, \varphi_{m2} = 4.4\ eV, \varphi_{m3} = 4.0\ eV, N_A = 1 \times 10^{16}, tsi = 20nm, t1 = 1nm, t2 = 2nm, V_{gs} = 0.5V, V_{DS} = 0.1V, L = 30nm, L1 = L2 = L3$.

As mentioned above, analytical solution of Schrodinger-Poisson's equation using variational approach is utilized to achieve the center and surface potential of TMG-CGS MOSFET's with high-k oxide. The proposed analytical model is verified and calibrated by plotted graph of electric field in MATLAB and compared with the results earned from numerical TCAD device simulator ATLAS [15], which are shown in Fig. 2 .

4. Results and Discussion

In this section, the analytical and analysis modelingare discussedfor a channel length, L=30 nm, device radius, r=t_{si}/2=20 nm, uniformly doped source/drain, $N_D$with doping density of 1×10^{20} cm^{-3}, The channel is kept lightly doped with doping density of $N_A = 1 \times 10^{16}$ cm^{-3}, SiO_2 thickness, t1=1nm, high-K dielectric thickness, t2=2 nm, dielectric constant of SiO_2, $\epsilon_1 = 3.9$, dielectric constant of high-K dielectric, like HfO2/La2O3, $\epsilon_2 = 20$, The work function of the gate materials in decreasing order from source to drain are (φ_{m1}) is 4.8 eV (Au), gate material 2 with (φ_{m2}) is 4.6 eV (Mo) and gate material 3 with (φ_{m3}) is 4.4 eV (Ti). Also, results obtained from theoretical models of natural length, the center potential and the sub- threshold swings are compared with the numerical simulation results.

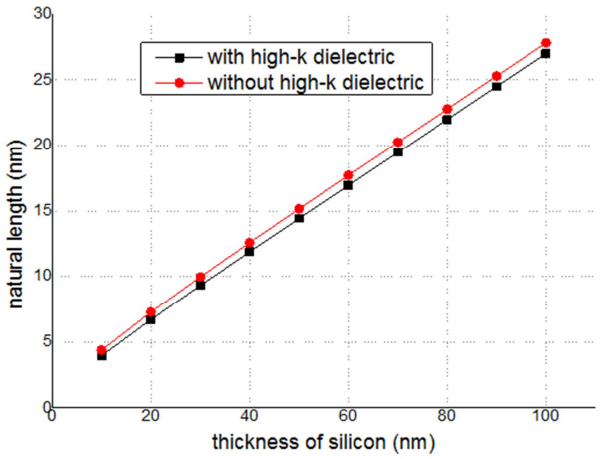

Fig. 3. Comparison between the natural lengthsalong Silicon thickness for high-k TMG-CGS MOSFET's and without high-k TMG-CGS MOSFET's devices, using: $\varphi_{m1} = 4.8eV, \varphi_{m2} = 4.6\ eV, \varphi_{m3} = 4.4\ eV, N_A = 1 \times 10^{16}, tsi = 20nm, t1 = 1nm, t2 = 2nm, V_{gs} = 0.1V, V_{DS} = 0.1V$.

Fig. 3 shows the variation of natural length along Silicon thickness for high-k TMG-CGS MOSFET's and without high-k TMG-CGS MOSFET's devices, at *Vgs*=0.1 V and Vds=0.1 V. The result shows that the natural length associated with the proposed center potential model with high-k dielectric is smaller than the natural length estimated by proposing in SarveshDubey et al. [3]. This concludes that the model works well to provide not only extremely thin layer of SiO_2 and high-k oxide with together are used as a coating to reduce the interface trap density but also can increase the device performance.

Fig. 4 and Fig. 5 show the relation between the ratio of channel length to natural length (L/λ_c) for various values of silicon film thickness and sub-threshold slope versus that ratio (L/λ_c) in different thickness of oxide and high-k, respectively. As silicon film thickness is scaled down, L/λ_c ratio increases to a greater extent in high-k TM surrounding / cylindrical gate MOSFET as compared to conventional state. As we know, the large value of L/λ_c is responsible for smaller sub-threshold swing and better short channel performance [2], [16].

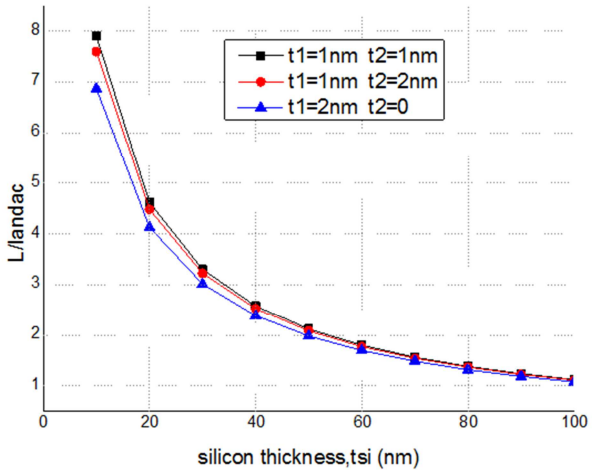

Fig. 4. Variation of ratio of channel length to natural length with silicon film thickness for TM-surrounded gate MOSFET with and without high-k oxide.

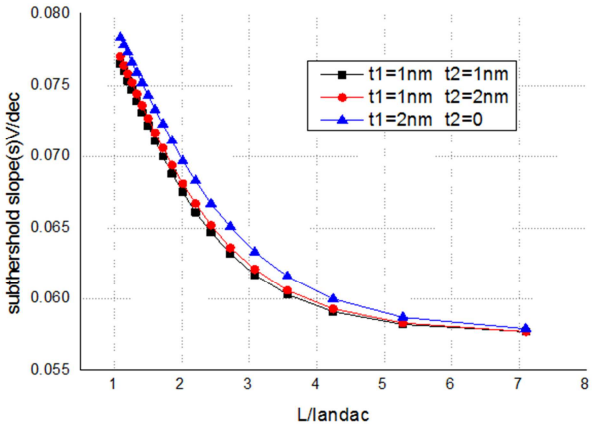

Fig. 5. Subthreshold slope of TMG-CGS MOSFET versus the $L/\lambda_c$for various tox and t2.

Fig. 6 shows sub-threshold slope versus dielectric constant of the upper gate dielectric (ϵ_2) for TMG-CGS MOSFET's with high-k oxide. The value of dielectric constant of the lower gate dielectric is 3.9. According to that, sub-threshold slope decreases with an increase in the dielectric constant for the upper dielectric layer. This is because, with an increase in

dielectric constant of the upper oxide, ϵ_2, the effective potential at the center and surface increases leading to a reduction in sub-threshold slope [6,9].

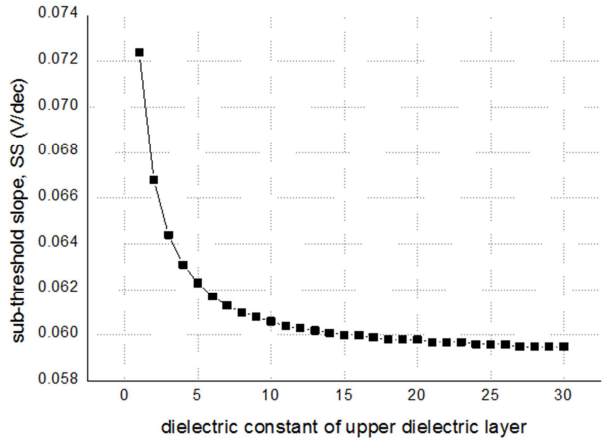

Fig. 6. Variation of sub-threshold slope, SS, as a function of dielectric constant of upper dielectric layer(ϵ_2)for TMG-CGS MOSFET, with high-k oxide.

In Fig. 7 the variation of center potential curve along the channel length for different values of the drain voltage has been shown for TMG-CGS MOSFETs with high-k oxide. It can be seen that the minimum potential level transfers to higher level with the increasing drain voltage, which is due to the presence of the DIBL effect. Fig. 8 shows the center potential curve versus the channel length for various gate length ratios of L1:L2:L3. It can be observed that the level of the minimum potential point move to up and toward the source side with increasing the length of the screen gates. As predicted in [3] the DIBL reduces as screen gate length increases, which is due to the shift in the minimum potential point away from the drain. But at the same time, other short-channel effects rise due to the lesser control gate length and its lesser control over the channel.

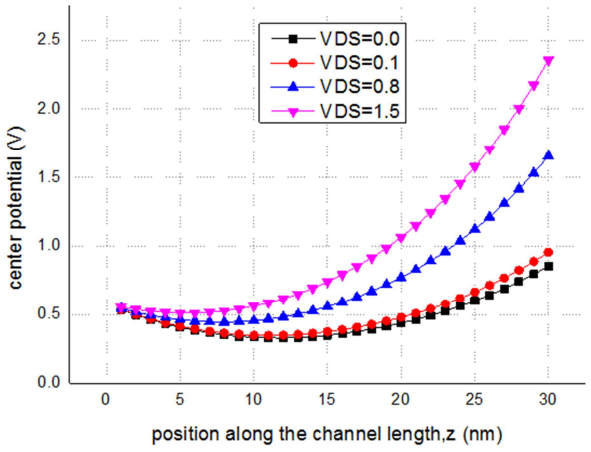

Fig. 7. Center potential variation for the Triple metal cylindrical surround gate MOSFET with high-k oxide for different values of VDS and VGS=0.1 V.

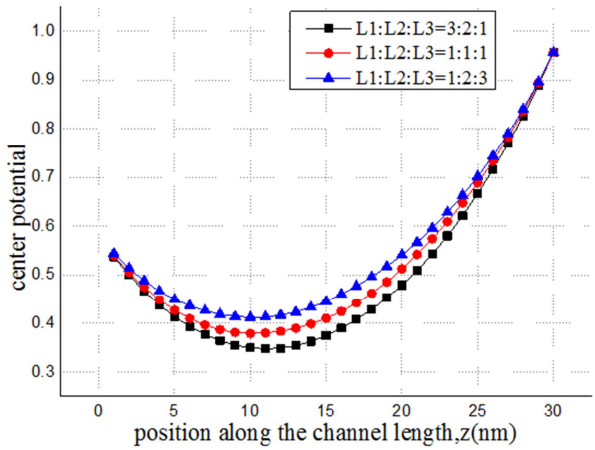

Fig. 8. Center potential along the channel length at various gate length ratios L1: L2: L3 . Parameters used: $\varphi_{m1} = 4.8eV, \varphi_{m2} = 4.6\ eV, \varphi_{m3} = 4.4\ eV, N_A = 1 \times 10^{16}, tsi = 20nm, t1 = 1nm, t2 = 2nm, V_{gs} = 0.1V, V_{DS} = 0.1V$.

Fig. 9 shows the variation of center potential of TMG-CGS MOSFET with and without high-k material along the channel. It can be observed that the center potential point decreases with the increase in thickness of high-k dielectric material. The substantial decrease in center potential with high-k dielectric material in comparison to gate without high K dielectric material is also evident. Therefore, use of high-k dielectric material with higher thickness with respect to SiO_2 leads to better gate controllability.

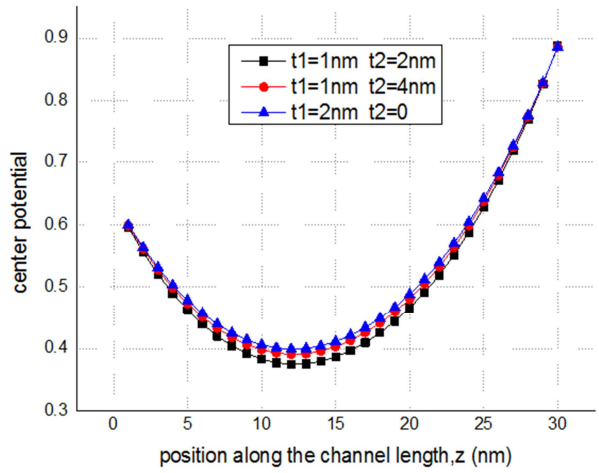

Fig. 9. Center Potential along the channel for different values tox and t2. Parameters used $\varphi_{m1} = 4.8eV, \varphi_{m2} = 4.6\ eV, \varphi_{m3} = 4.4\ eV, N_A = 1 \times 10^{16}, tsi = 20nm, V_{gs} = 0.1V, V_{DS} = 0.1V$.

5. Conclusions

An analytical based center potential model for a Triple metal cylindrical surround gate MOSFET with high-k material over silicon oxide is derived and the effects of device properties have been studied. From the results, it can be concluded that the high-k material on SiO_2 can improve device characteristic in the TM-CGS compared with TM-CGS without high-k

material. The reductions in natural length, sub-threshold swing, and minimum point of center potential are the effect of this structure. Also with introduce triple high-k material and using moderately doped, when the screen gate length increased, the impact of DIBL is reduced. The substantial decrease in center potential with high-k dielectric material in comparison to gate without high-k dielectric material is also clear. Therefore, using high-k dielectric material instead of SiO_2 leads to better gate controllability. Though, it may occur that the device performance is reduced due to the increased fringing fields from the gate to the source/drain regions, but a trade off between gate lengths, SCEs, DIBL and high-k material oxide on SiO_2 can be useful to optimize the device performance.

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