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Design of a High Linear CMOS Power Amplifier for Ultra-Wideband Applications Using the Derivative Superposition Method

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Abstract

The problem with the power amplifiers is that raising the gain and output power may affect the other amplifier factors specially in the frequency ultra-band. This paper presents a CMOS power amplifier (PA) for Ultra-Wideband (UWB) applications in 2.2 to 5 GHz using two stages of common source topology with derivative superposition (DS) method. Simulation results show an average power gain of 27.2 dB with an input 1dB compression point (1dB-CP) of -14.6 dBm at 3.2 GHz and an output 1dB compression point (1dB-CP) 12.9 dBm. With an input power of 83.8 mW, from a 1.8 V supply, power added efficiency (PAE) is 47.5% at 3.2 GHz with 50Ω load impedance and stability factor is 7.2 at 3.2GHz. The proposed design has been simulated using TSMC 0.18µm technology. The important parameters that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. The design results showed high power output without affecting the other amplifier factors. A comparison with the previous research has been done and the comparison is clearly in favor of the present design.

Keywords

Ultra-Wideband (UWB), Power Amplifier (PA), Derivative Superposition (DS) Method, Common Source Power Amplifier

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1. Introduction

a. Scope

The goal of this research is to design Power Amplifier in an integrated circuit. It is focused on RF Power Amplifier design in 2.2 to 5 GHz frequency band which is suitable for using for Ultra-Wideband (UWB) wireless communication system, In order to keep pace new competitive communication technology.

b. Problem Overview

Many of today's communication devices, especially mobile devices, require high performance, low power consumption ICs to insure steady connectivity and longer battery life. The development of digital devices goes from small to smaller, which needs minimizing the sizes of ICs as possible. One of the best ways to meet this is by fully integrating the communication circuit in one single chip. This would lead to smaller size, lower power consuming and greater performance. The Radio Frequency (RF) power amplifier (PA) is a type of electronic amplifier used to convert a low-power radio-frequency signal into a larger signal of significant power, typically for driving the antenna of a transmitter.

The RF power amplifier plays an important role in RF systems. It is used as a final stage of a transmitter to provide signal power to a transmitting antenna. The basic techniques for RF power amplification can use classes as A, B, C, D, E, and F. The RF Output Power can range from a few mW to MW, depending on applications. Most important parameters

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that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. The values of these parameters are high or low depending on the applications that uses the RF-PA such as ultra-wideband (UWB) [1]. Figure 1 presents the block diagram of the general RF transceiver. The problem with the power amplifiers is that raising the gain and output power may affect the other amplifier factors specially in the frequency ultra-band.

This paper introduces the design and simulation of common source wide band power amplifier. Also, it presents and simulates the Common Source Power Amplifier with derivative superposition (CS PA with DS) design method. The present design is done in the band (2.2 – 5.0) GHz. Most important parameters that define an RF Power Amplifier are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. This paper presents these factors as well as the different classes of power amplifier. The present design results showed high power output without affecting the other amplifier factors. A comparison with the previous research has been done and it shows that the paper results are much better than the results of these research works. The paper has 6 sections. Section (1) is an introduction and section (2) is a background about RF-PA including how to run the PA, the power amplifier parameters, the amplifier classes, and the tow-port network of the RF-PA (S-Parameters). Section (3) depicts some of the literature review about the topic and section (4) illustrates the simulation of the RF-PA including the common source power amplifier and the common source power amplifier with derivative superposition (CS PA with DS) design method. Section (5) presents the simulation results for both the cases and section (6) introduces a discussion and comparison with the previous work. Section (7) gives some conclusions and a list of the used references is given at the end of the paper.

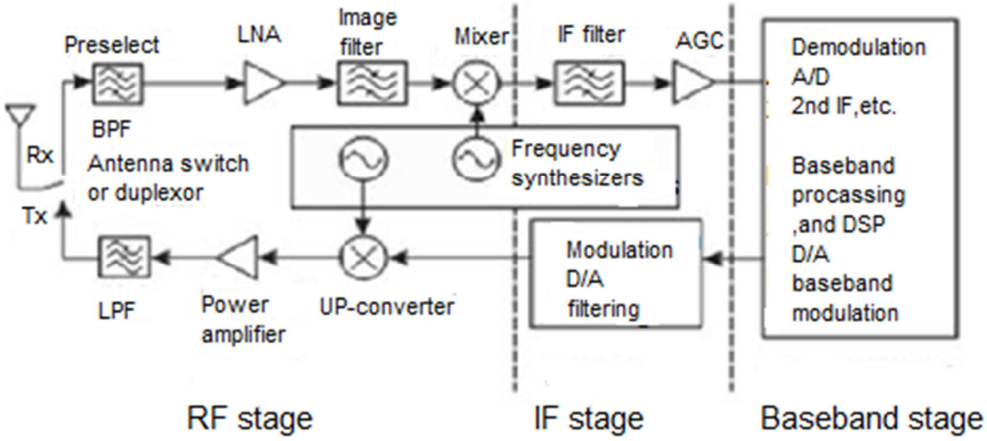

Figure 1. Block diagram of the general RF transceiver [2].

2. A Background About RF-PA

2.1. How to Run the PA

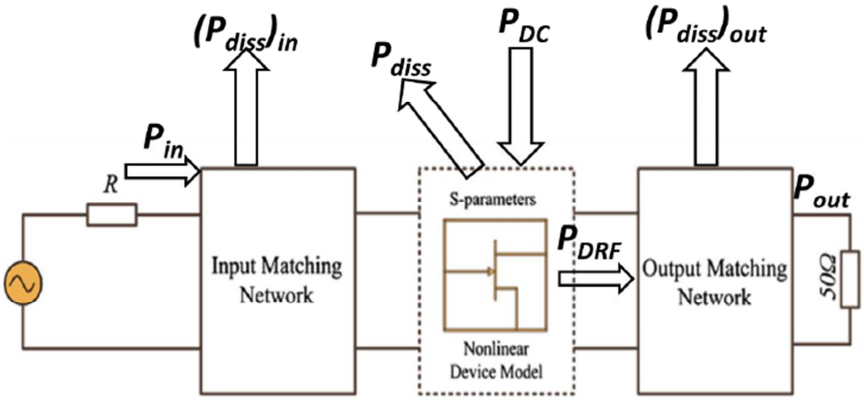

Figure 2. The power flow in power amplifiers [3].

Figure 2 shows the power flow through the PA, where P_{in} is the input power from the source at the wanted frequency, and

the P_{out} is the output power from the PA to the load. The RF input signal (P_{in}) is received through the input port passing through the input matching circuit to the active device. The input matching network dissipates some of the input power as a heat, and sends the remaining part to the active device. The input RF power P_{in} and the input DC power PDC are fed to the nonlinear active device which dissipates portion of the power P_{diss} as heat, and the remaining part P_{DRF} are transferred to the output matching network. The output matching network also dissipates some of the power as a heat, and delivers the remaining part to the 50 Ohms load. The dissipated power through the matching networks and the nonlinear active device degrade the efficiency of the PA [3].

2.2. Power Amplifier Parameters

a. Output power:

The output power (P_{out}) can be defined as the amount of power a component, circuit or system (usually amplifier) can send to a load. Good input and output impedance matching is necessary to reduce the losses to increase the output power. The amount of output power depends mainly on the applications [1].

b. Power gain and gain flatness:

The power gain is defined as the mean ratio of the signal output of the amplifier to its signal input. Power gain, in decibels (dB), is defined flowing:

$$Gain = 20 \log \left(\frac{P_{out}}{P_{in}}\right) dB \quad (1)$$

Where P_{in} and P_{out} are the input and output powers respectively. Gain Flatness is a measure of the uniformity of the gain over the frequency band of interest. For PA's, it is desired that the gain of the amplifier to be flat across the frequency range, typically with ±10% tolerance. Gain flatness affects group delay variations largely.

c. Efficiency:

Efficiency measures the ability of the PA of transforming the DC power to RF output power [4]. Using the power flow through the PA shown in Figure 2, the drain efficiency is the ratio between the RF output power (P_{out}) and DC power (P_{DC}) [5], η_D *is*:

$$\eta_D = \frac{P_{out}}{P_{DC}} \quad (2)$$

There is also have the power added efficiency (PAE) which takes the gain of the amplifier into account and it is defined as [5]:

$$PAE = \frac{P_{out} - P_{DC}}{P_{in}} \quad (3)$$

Rearranging the PAE equation in terms of gain as following [4]:

$$PAE = \frac{P_{out}}{P_{DC}}\left(1 - \frac{P_{in}}{P_{out}}\right) = \eta_D \left(1 - \frac{1}{G}\right) \quad (4)$$

where *G* is the power gain of the PA.

Total efficiency (η_{total}) is defined as the ratio between the RF output power to the summation of DC power and RF input powers which are fed to the nonlinear active device. The expression for η_{total} can be written as following:

$$\eta_{total} = \frac{P_{out}}{P_{in} + P_D} \quad (5)$$

Both PAE and overall efficiency capture the effect of input power on power amplifier efficiency.

d. Linearity:

Linearity means simply that the dependent variable varies in direct proportion to the independent variable. When two or more signals are input to a nonlinear amplifier simultaneously, the second, third, and higher-order intermodulation components (IM) are caused by the sum and difference products of each of the fundamental input signals and their associated harmonics. When two perfect sinusoidal signals, at frequencies f1 and f2, are input to any nonlinear amplifier, the following output components will result, see figure 3 for illustration:

Fundamental: f1, f2

Second order: 2f1, 2f2, f1 +f2, f1 −f2

Third order: 3f1, 3f2, 2f1 ±f2, 2f2 ± f1 +higher order terms

Fourth order: 4f1, 4f2, 2f2 ± 2f1,

Fifth order: 5f1, 5f2, 3f1 ± 2f2, 3f2 ± 2f1, + Higher order terms

Under normal circuit operation, the second-, third-, and higher order terms are usually at a much smaller signal level than the fundamental component and, in the time domain, this is seen as distortion.

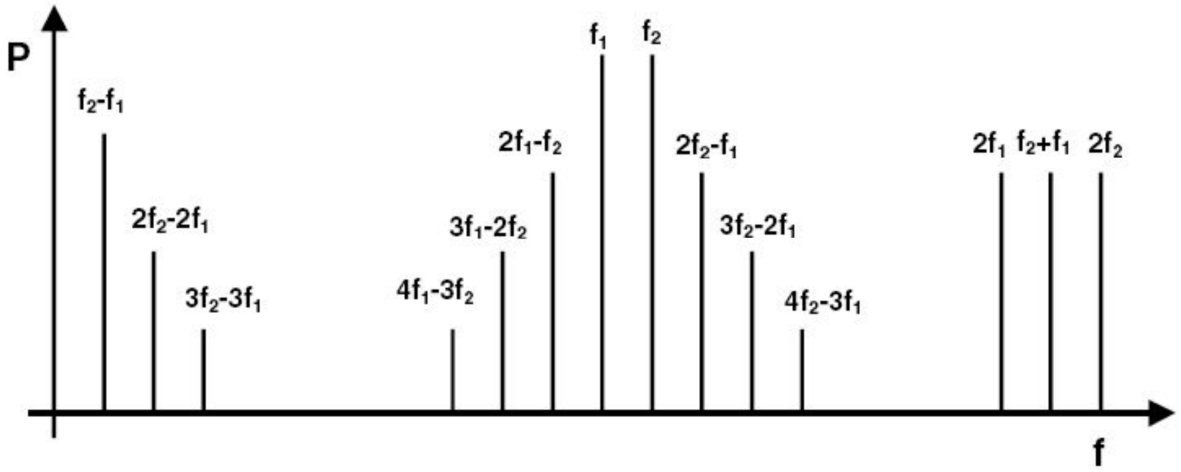

Figure 3. The signal fundamental frequency and harmonics.

e. Stability:

The system stability may be conditional stable (i.e., if its input and output reflection coefficients greater than one ($|\Gamma_{in}| > 1$ and $|\Gamma_{out}| > 1$) for a certain range of source and load passive impedances [6]) or unconditional (i.e., if the magnitude of the input and output reflection coefficients are fewer than unity ($|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$) for all passive source and load impedances ($|\Gamma_S| < 1$ and $|\Gamma_L| < 1$) [6]). The RF-PA must be unconditionally stable over the whole frequency band. Stability problems might cause system functionality change, such as amplifiers working as oscillators. The stability of two port networks, especially amplifiers, depend on their input and output reflection coefficients (Γ_{in}) and (Γ_{out}). Because of Γ_{in} and Γ_{out} dependence on Γ_S and Γ_L, the stability depends basically on the source and load terminations [6]. There are two different types of stability.

f. Ruggedness:

Is the ability to withstand electrical overstress without failure or degradation. The ruggedness is normally tested under some prescribed Conditions like output over voltage, input overdrive and mismatch load conditions.

2.3. Amplifier Classes

Consider the simplified NMOS power amplifier of Figure 4. The behavior of the amplifier is determined by the input signal, the load impedance and conduction angle. Power amplifiers can be divided into classes based on their achieved efficiency.

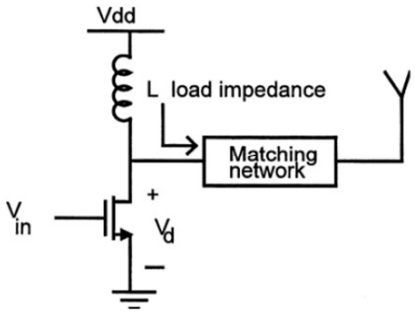

Figure 4. The simplified output stage of a RF power amplifier.

2.3.1. The Class-A power Amplifier

Figure 5 explains the behavior of the class-A power amplifier. In the following, some of the properties are given:

1. An amplifier that is biased so that the output current flows at all the time, and the input signal drive level is kept small enough to avoid driving the transistor in cut-off (The transistor of the amplifier is biased and driven so that it is always in active mode).
2. The conduction angle of the transistor is 360°, meaning that the transistor conducts for the full cycle of the input signal.
3. Class-A is the most linear of all amplifier types, where linearity means simply how closely the output signal of the amplifier similar to the input signal.
4. The maximum theoretically obtainable efficiency is 35% for resistive load and 50% for inductive load.
5. The absence of harmonics in the amplification process, allows Class-A to be used at frequencies close to the maximum capability (f_{max}) of the transistor.
6. Class-A PAs are therefore typically used in applications requiring low power, high linearity, high gain, broadband operation, or high-frequency operation.

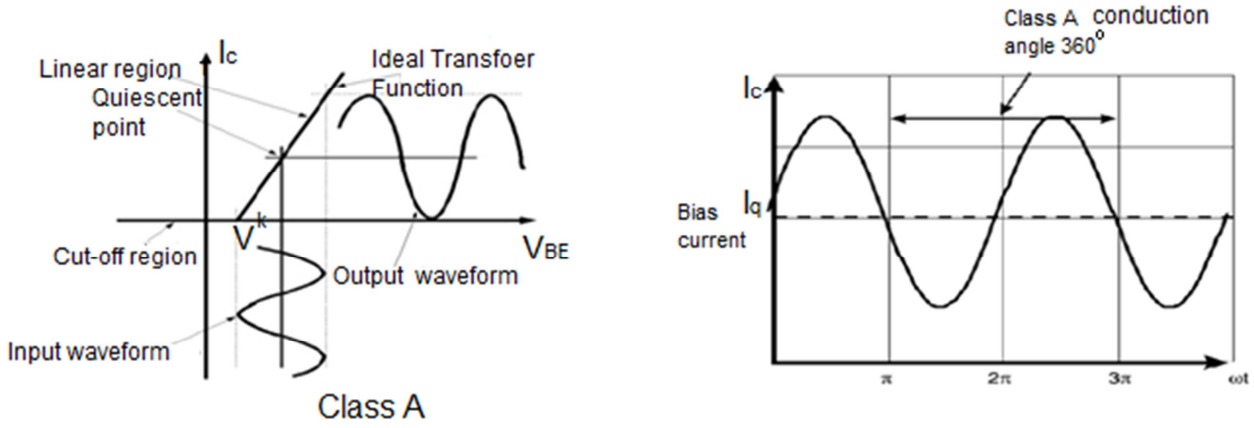

Figure 5. The Class-A power amplifier behavior.

2.3.2. The Class-B Power Amplifier

Figure 6 presents the class-B power amplifier behavior and in the following, some of the properties are given:

1. To increase the efficiency, the transistor can be made active only half of the time but this method increase distortion.
2. To still have low distortion levels, the bias currents are chosen to be small and the transistor is normally in its saturation mode.
3. The conduction angle for the transistor is approximately 180 degrees.
4. The transistor conducts only half of the time, either on positive or negative half cycle of the input signal.
5. Class-B amplifiers are more efficient than Class-A amplifiers.
6. The efficiency of a Class-B PA varies with the output voltage and for an ideal PA reaches π/4 (78.5%).
7. Common configuration of Class-B amplifier is push-pull amplifier.
8. In this configuration, one transistor conducts during positive half cycles of the input signal and the second transistor conducts during the negative half cycle. In this way, the entire input signal is reproduced at the output.

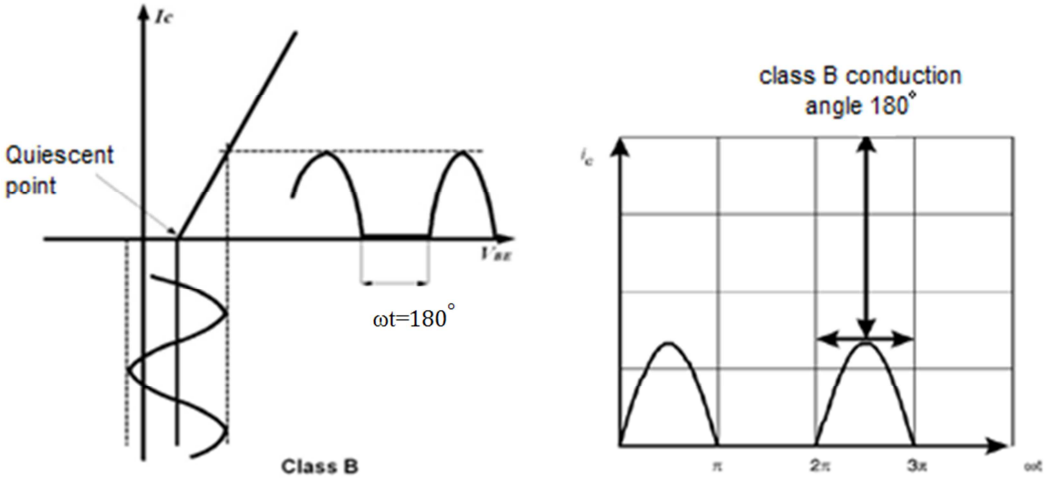

Figure 6. The Class-B power amplifier behavior.

2.3.3. The Class-AB Power Amplifier

This amplifier is a compromise between Class-A and Class-B in terms of efficiency and linearity. Figure 7 presents the behavior of the class-AB power amplifier and some of its properties are given as follows:

1. The transistor will be ON for more than half a cycle, but less than a full cycle of the input signal.
2. Conduction angle in Class-AB is between 180° and 360° and efficiency is between 50% and 78.5%
3. Class-AB has higher efficiency than Class-A at price of linearity.

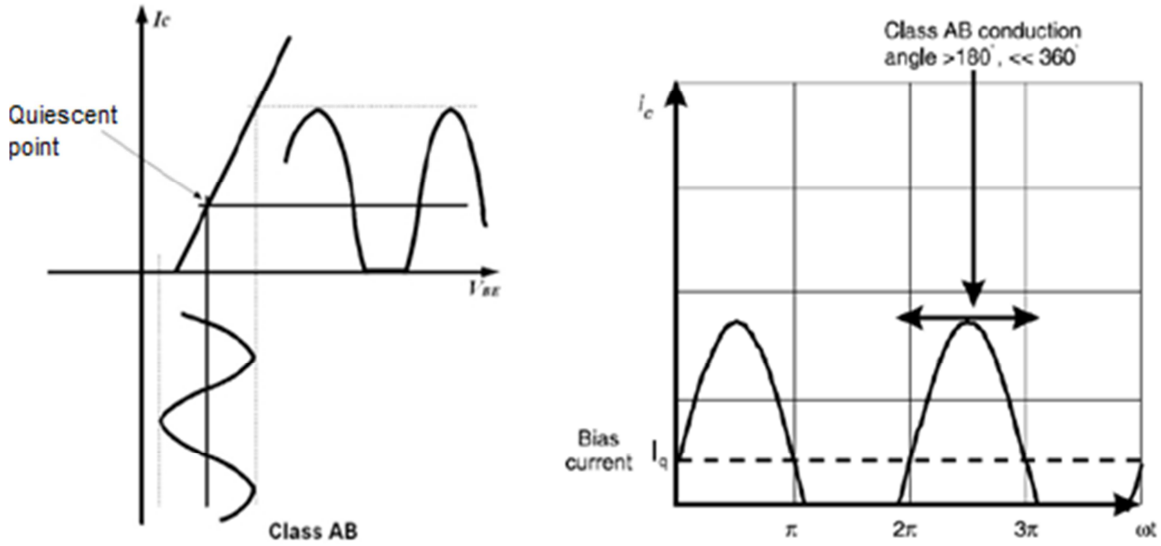

Figure 7. The class-AB power amplifier behavior.

2.3.4. The Class-C Power Amplifier

The class-C power amplifier is an amplifier where the conduction angle for the transistor is significantly less than 180°. Figure 8 presents its behavior and in the following, some of its properties are given:

1. The efficiency depends on the conduction angle and as the angle reduces the efficiency increases.
2. The output signal does not follow the input signal, the amplifier behaves non-linearly and the distortion levels are high.
3. Linearity of the Class-C amplifier is the poorest of the classes of amplifiers.
4. The Efficiency of Class-C can approach 85%, which is much better than either the Class-B or the Class-A amplifier.

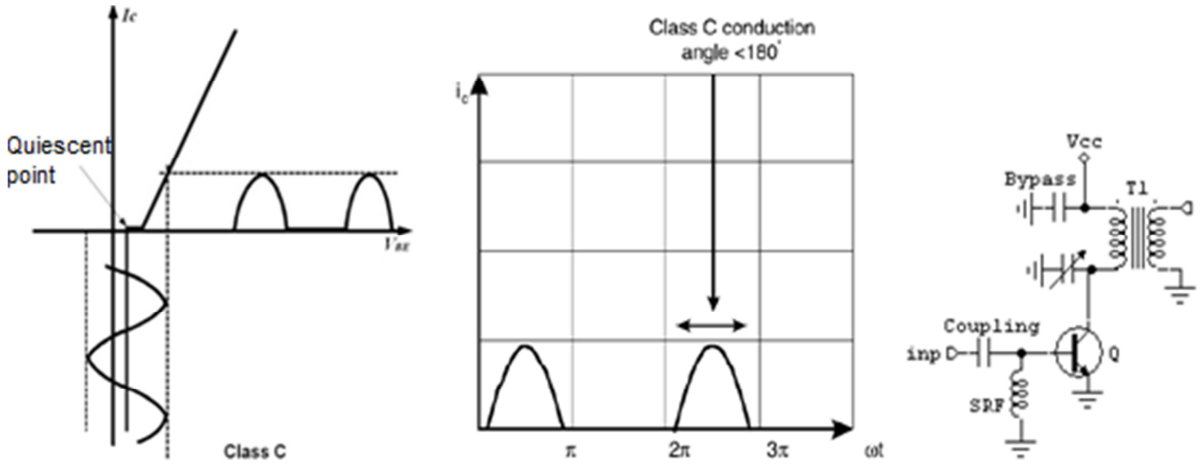

Figure 8. The behavior of class-C power amplifier.

2.3.5. The Class–D Power Amplifier

It is defined as a switching circuit that results in the generation of a half-sinusoidal current waveform and a square voltage waveform. Figure 9 presents the behavior of the class-D power amplifier and in the following, some of its properties are given:

1. Use two or more transistors as switches to generate a square drain-voltage waveform, but neither is forced to simultaneously support both voltage and current.
2. One can reach 100% efficiency, but in practical applications the efficiency is comparable to Class C.
3. The disadvantage of class D compared to Class C is in the synchronization of the two (or more) switches.

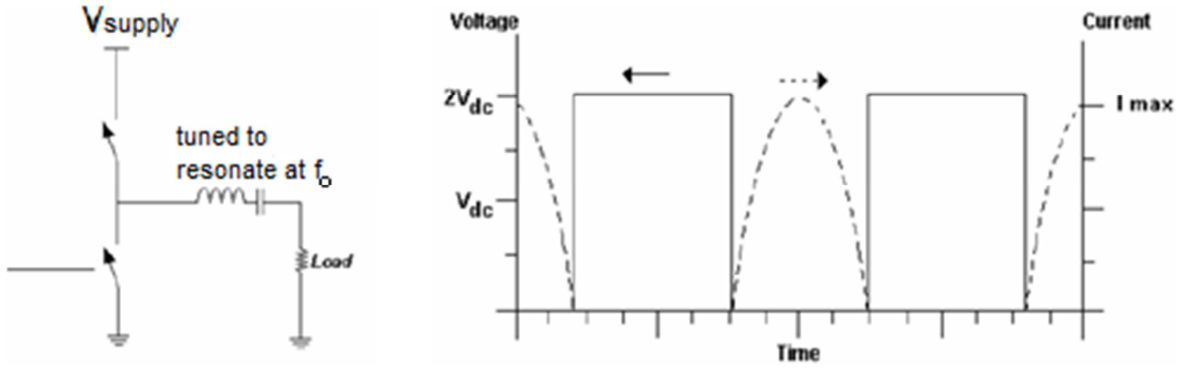

Figure 9. The behavior of the class-D power amplifier.

2.3.6. The Class-E Power Amplifier

This class employs a single transistor operated as a switch. Figure 10 explains the amplifier behavior and in the following, some of its properties are given:

1. A resonance network is used to allow switching when the voltage is low.
2. The switching device, i.e. the power transistor, becomes active when the slope of the voltage and current are either almost zero or almost zero.
3. Consequently, even with mistiming, the loss is low and therefore high efficiency rates can be achieved.
4. The resonance network is placed between the output of the transistor and the load, and the resonance frequency is at the fundamental RF frequency.
5. This class of operation is most often used in RF mobile transmitters.

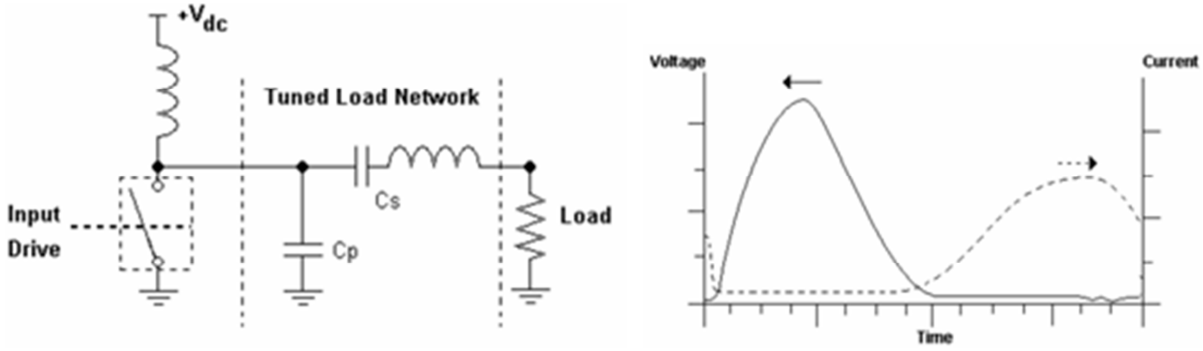

Figure 10. The class-E power amplifier behavior.

2.3.7. The Class-F Power Amplifier

If the single switch of class-C is combined with the square wave voltage approach of class-D, class-F is obtained. Figure 11 depicts the behavior of the class-F power amplifier and in the following, some of its properties are given:

1. A resonance circuit at the third harmonic of the RF frequency is placed at the output of the single transistor to flatten out the voltage and "shape" it like a square wave voltage.
2. The voltage waveform includes one or more odd harmonics and approximates a square wave, while the current includes even harmonics and approximates a half sine wave.

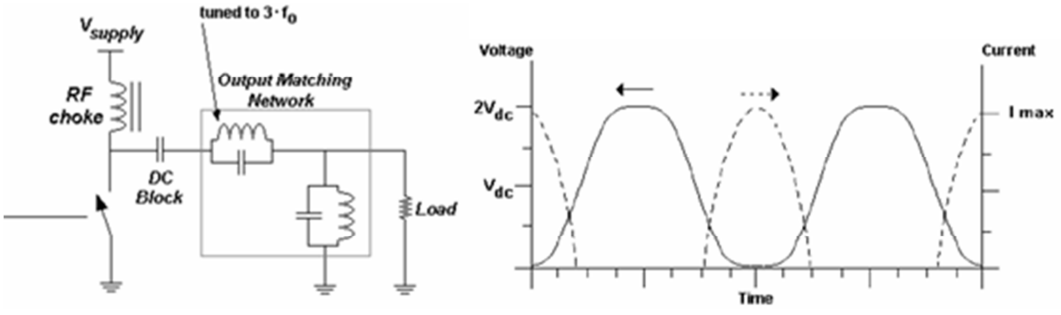

Figure 11. The behavior of the class-F power amplifier.

Figure 12 defines the power amplifier classes based on the conduction angle and the signal overdrive. For small input signals, the RF PA can operate in class A, AB, B or C, depending on the conduction angle. The conduction angle is determined primarily by the DC gate bias. The efficiency can be improved by reducing the conduction angle and moving in the direction of class C at the expense of lower output power. An alternative is to increase the gate overdrive until the PA operates as a switch, while keeping the same conduction angle.

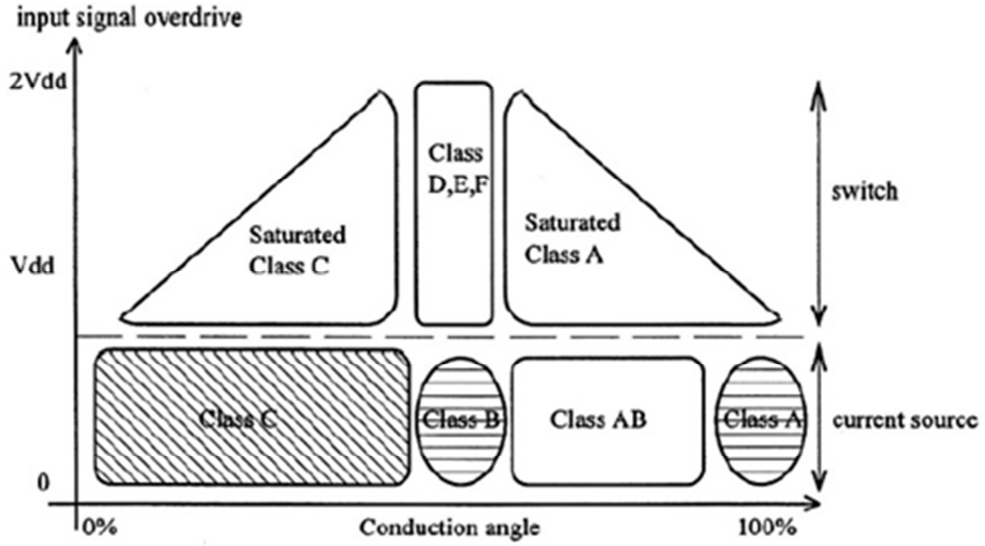

Figure 12. Definition of PAs based on conduction angle and signal overdrive.

2.4. Tow-Port Network of the RF-PA (S-Parameters)

2.4.1. Determining the Values for S-Parameters

Scatter Parameters or S-Parameters are two port network parameters used in the two port network theory. They relate to the travelling waves that are scattered or reflected when a network is inserted into a transmission line of a certain characteristic impedance. The S-Parameters are important in the microwave design because they are easier to measure and to work with in high frequencies than any other kind of two port network parameters. They are conceptually simple, analytically convenient, and capable to provide a detailed insight into measurements and modeling problems. The S-Parameters represent the linear behavior of the two ports as shown in figure 13 [7].

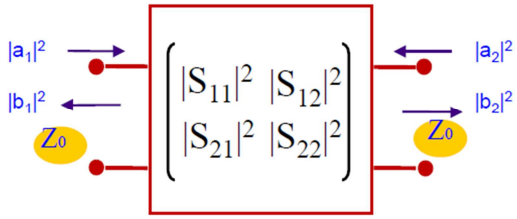

Figure 13. S-Parameters in two-port network

$|a_1|^2$: power travelling towards port 1, $|a_2|^2$: power travelling towards port 2.

$|b_1|^2$: Power reflected from port 1, $|b_2|^2$: Power reflected from port 2.

Figure 14 explains the elements of the S-Parameters. Thus, these elements can be obtained as follows:

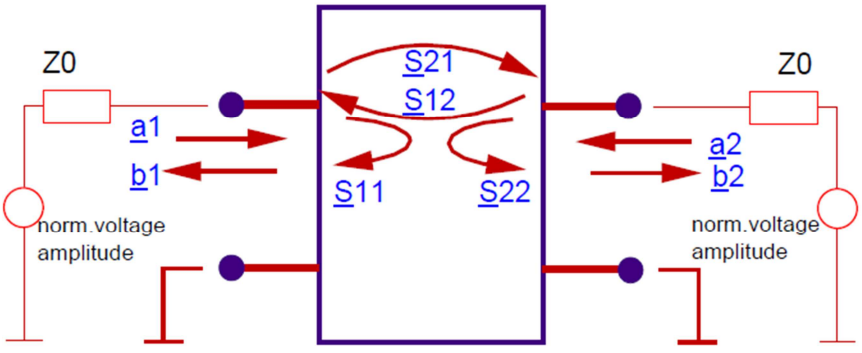

Figure 14. Elements of S-Parameters.

$$S11 = \left(\frac{b1}{a1}\right)_{a2=0} = \left(\frac{V_{reflected\ at\ port\ 1}}{V_{towards\ port\ 1}}\right)_{a2=0} \text{ Representing the input matching} \quad (6)$$

$$S12 = \left(\frac{b1}{a2}\right)_{a1=0} = \left(\frac{V_{out\ of\ port\ 1}}{V_{towards\ port\ 2}}\right)_{a1=0} \text{ Representing the forward gain} \quad (7)$$

$$S21 = \left(\frac{b2}{a1}\right)_{a2=0} = \left(\frac{V_{reflected\ at\ port\ 2}}{V_{towards\ port\ 1}}\right)_{a2=0} \text{ Representing the reverse gain} \quad (8)$$

$$S22 = \left(\frac{b2}{a2}\right)_{a1=0} = \left(\frac{V_{reflected\ at\ port\ 2}}{V_{towards\ port\ 2}}\right)_{a1=0} \text{ Representing the output matching} \quad (9)$$

It can also be written:

$$P = V * I \rightarrow P = V * \frac{V}{Z_0} \rightarrow \sqrt{P} = \frac{V}{\sqrt{Z_0}} = I * \sqrt{Z_0} \quad (10)$$

Thus, the power can be converted towards the two-port into normalized voltage amplitude of:

$$a_1 = \frac{V_{Towards\ port\ 1}}{\sqrt{Z_0}}, a_2 = \frac{V_{Towards\ port\ 2}}{\sqrt{Z_0}} \quad (11)$$

and the power can be converted away of the two-port into normalized voltage too:

$$\therefore b_1 = \frac{V_{away\ from\ port\ 1}}{\sqrt{Z_0}}, b_2 = \frac{V_{away\ from\ port\ 2}}{\sqrt{Z_0}} \quad (12)$$

2.4.2. Stability with S-Parameters

The tendency of a transistor towards oscillation can be gauged by its S-parameter data. The calculation can be made even before an amplifier is built up and, thus, it serves as a useful tool in finding a suitable transistor for the application. To calculate the stability of a transistor with S parameters, the intermediate quantity *DS* must be first calculated:

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \quad (13)$$

The Rollett Stability Factor (*K*) is then calculated as:

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \quad (14)$$

If *K* is greater than 1, then the device will be unconditionally stable for any combination of source and load impedance. If, on the other hand, *K is l*ess than 1, the device is potentially unstable and it will most likely oscillate with certain combinations of source and load impedance. With *K* less than 1, care must be extremely taken in choosing source and load impedances for the transistor. It does not mean that the transistor cannot be used for the application. It merely indicates that the transistor will be more difficult to use.

3. A Literature Review

Many topologies have been used in the implementation of these UWB power amplifiers. These topologies include the common source (CS) inductive degeneration, the derivative superposition [8] and the cascaded common source (CS) structure [9]. Normally, the design requirements of the amplifier such as bandwidth, gain, PAE and linearity basically determine the most suitable configurations. In this section, a brief summary of the properties of these topologies is given.

Yilei et. al. offered two-stage of derivative superposition get high gain and good linearity but poor power added efficiency. [8]. Wong et. al. offered a two-stage cascaded common source to get higher gain, good wide bandwidth, good linearity and low power consumption but poor power added efficiency. [9]. Alegre offered common source power amplifier to get high gain and good linearity but poor power added efficiency. [10]. Vu et. al. offered two-stage cascade common source power amplifier to get high gain and high linearity but poor power added efficiency. [11]. Mosalam offered two-stage cascade common source power amplifier to get good gain and good linearity but poor power added efficiency [3].

4. Simulation of the RF-PA

4.1. Common Source Power Amplifier

In this design, a PA has two stage amplifiers to get the required gain and output power. The first stage consists of a current mirror for biasing (MC1) and a cascade common source to get high gain. The biasing circuit is a current mirror with the width is about 6µm. Elements R1, R2, Ls1 are used for linearity and stability. About "180pH" Lg1 is needed for impedance matching and about "180pH" Ld1 is used as a shunt peaking inductor. About "4nH", C1, C2, C3 are used for RF shunting. The main transistor M1 in the first stage amplifies the signal. To calculate the size of the transistor M1, the following equation is used:

$$I_{DD} = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_t)^2 \quad (15)$$

where $V_{GS1} = 0.8V, V_t = 0.5V$, $\mu_n = 0.03903\ m^2/\mathrm{V-s}$, and $C_{ox} = 0.00946\ F/m^2$, for a typical -0.18 μm silicon CMOS process. The requisite trans-conductance (g_{m1}) can be additionally determined by the next equation [5]:

$$g_{m1} = \frac{\partial I_{DD}}{\partial V_{GS}} = 2\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right](V_{GS1} - V_t) \quad (16)$$

Reorganizing (15) to be $(V_{GS1} - V_t) = \sqrt{I_{DD}/\left[0.5\mu_n C_{ox}\frac{W}{L}\right]}$ and replacing it into equation (16), the equation for g_{m1}can be simplified to:

$$g_{m1} = 2\sqrt{0.5\mu_n C_{ox}\frac{W}{L}I_{DD}} = \sqrt{\beta . I_{DD}} \quad (17)$$

where $\beta = 0.5\mu_n C_{ox}\frac{W}{L}$ is well-known as trans-conductance parameter. The width of M1 is found to be about 184 µm and the width of Mb is found to be about 80 µm.

The second stage consists of a current mirror for biasing and a simple common source without cascade to get high gain as shown in figure 15. This PA gives a total dc power of 77.22mW from a 1.8V dc supply and total drain current of about 42.9mA. This stage has a biasing circuit of MC2 current mirror with a width of about "6µm". The elements R3, R4, Ls2 are used for linearity and stability enhance. About "180pH" Ld2 is used as a shunt peaking inductor. About 4nH", C4, C5 are used to RF shunting, and M2 is the main transistor in second stage that amplifies the signal using equations (15-17) to determine the width of about 184µm. The elements Cin, Cint, Cout are used for dc blocking. Cadence software has been used to design the circuit and make the simulation.

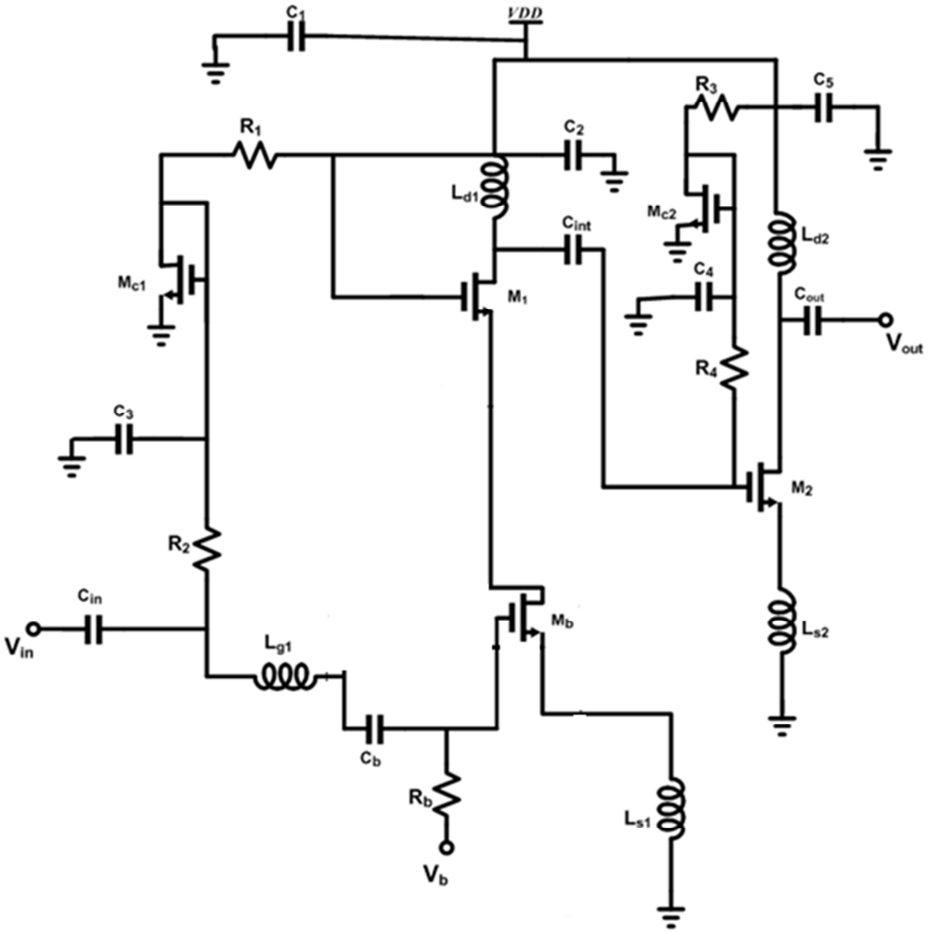

Figure 15. The circuit diagram of the two-stage CS PA.

4.2. Common Source Power Amplifier with Derivative Superposition (CS PA with DS) Design Method

In this design, a PA has two stage amplifiers to get the required gain and output power. The first stage consists of current mirror for biasing, common source to get high gain and derivative superposition method to get high linearity. Second stage consists of current mirror for biasing and simple common source to get the high gain as shown in figure 16. This PA gives total dc power 83.8mW from a 1.8V dc supply and total drain current of about 46.6mA.

The first stage consists of biasing circuit (MC1 current mirror "width is about 6µm", R1, R2, Ls1 "used for linearity and stability advance, it is about 180pH", Lg1 (needed to impedance matching, it is about 180pH", Ld1 (used as a shunt peaking inductor it is about 4nH", C1, C2, C3 (used for RF shunting", M1 (the main transistor in the first stage that amplify the signal). To calculate the size of transistor M1 the following equation is used:

$$I_{DD} = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_t)^2 \quad (18)$$

where $V_{GS1} = 0.8V, V_t = 0.5V$, $\mu_n = 0.03903\ m^2/\mathrm{V-s}$, and $C_{ox} = 0.00946\,F/m^2$, for a typical -0.18 μm silicon CMOS process. The requisite trans-conductance (g_{m1}) can be additionally determined by the next equation [5]:

$$g_{m1} = \frac{\partial I_{DD}}{\partial V_{GS}} = 2\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right](V_{GS1} - V_t) \quad (19)$$

Reorganization (18) to $(\mathrm{V_{GS1}} - \mathrm{V_t}) = \sqrt{\mathrm{I_{DD}}/\left[0.5\mu_n \mathrm{C_{ox}}\frac{\mathrm{W}}{\mathrm{L}}\right]}$ and replacing into (19), the equation for g_{m1} can be simplified to:

$$g_{m1} = 2\sqrt{0.5\mu_n C_{ox}\frac{W}{L}I_{DD}} = \sqrt{\beta . I_{DD}} \quad (20)$$

where $\beta = 0.5\mu_n C_{ox}\frac{W}{L}$ is well-known as trans-conductance parameter.

The width of M1 is determined as about 184 µm. At finally, the first stage containing the derivative superposition consists of two parallel transistors (Ma and Mb) and a biasing circuit (Ra, Rb, Ca, Cb, Va and Vb). Va is the voltage that biases Ma in sub-threshold and Vb is the voltage that biases Mb in a strong inversion region [12].

The second stage consists of a biasing circuit (MC2 current mirror "width is about 6µm", R3, R4, Ls2 "used for linearity and stability enhance, it is about 180pH", Ld2 "used as a shunt peaking inductor, it is about 4nH", C4, C5 "used for RF shunting", and M2 "the main transistor in second stage that amplifies the signal using equations (18-20) to determine the width as about 184µm"). Cin, Cint, Cout are used for dc blocking.

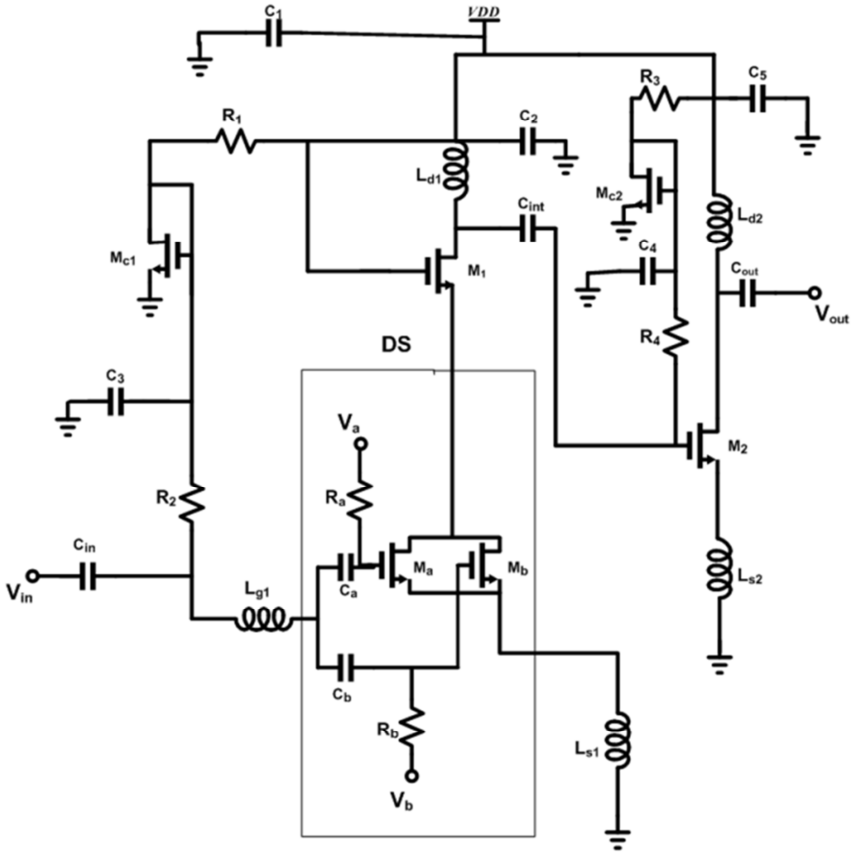

Figure 16. The circuit diagram of the two-stage CS PA with DS.

5. Simulation Results

5.1. Simulation Results for CS PA

5.1.1. S Parameter

The PA is designed using TSMC 0.18µm technology. The simulation is achieved using Cadence and based on the device models provided by this technology. This PA operates at 2.2 to 5GHz under 1.8V voltage supply. Figure 17 shows the scattering functions S11, S21, S12, and S22. Table 1 shows the value of scattering functions S11, S21, S12, and S22 at 3.2 GHz.

Table 1. The value of scattering functions at 3.2 GHz.

Function	Frequency	Value
S11	3.2 GHz	-1.3 dB
S12	3.2 GHz	-46.5 dB
S21	3.2 GHz	15.5 dB
S22	3.2 GHz	-10.3 dB

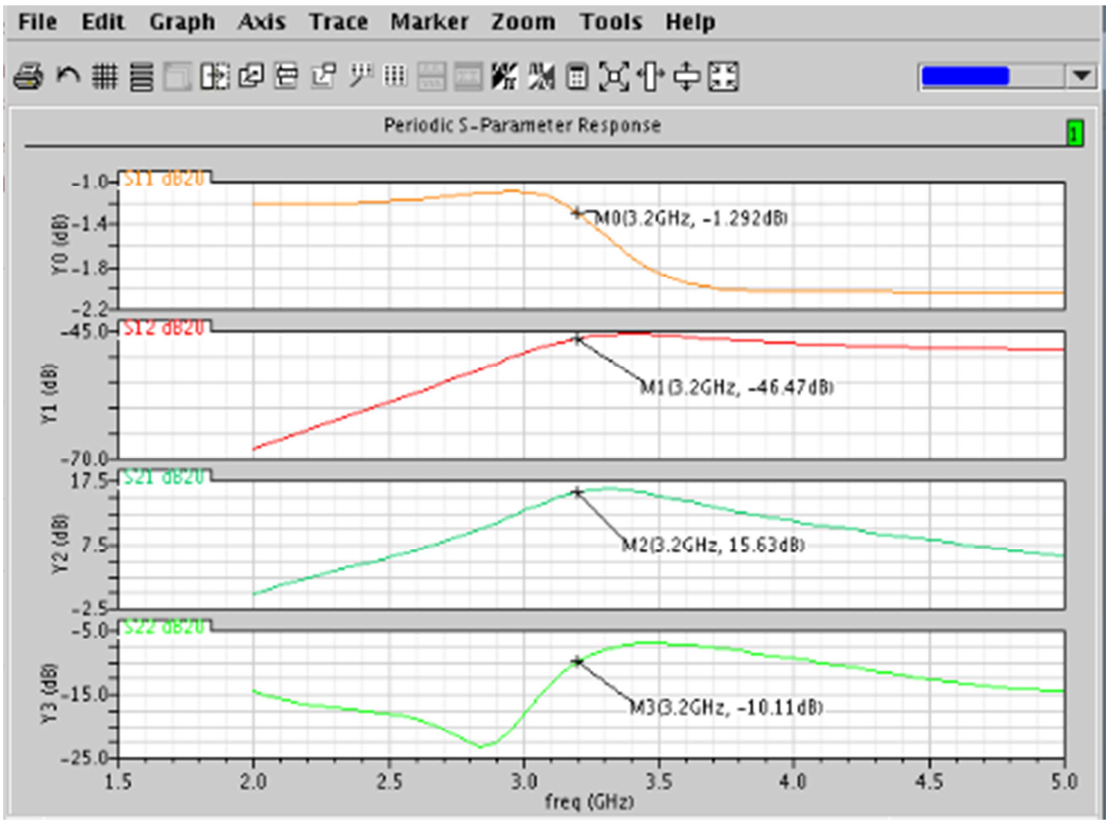

Figure 17. The scattering functions S11, S21, S12, and S22.

5.1.2. Stability Analysis of the CS PA

The S-parameter simulation is used to measure stability of the transistor by the stability factor (KF) where its value should be more than one. Figure 18 shows a good value of the stability factor (KF) is about 3.8 at 3.2GHz.

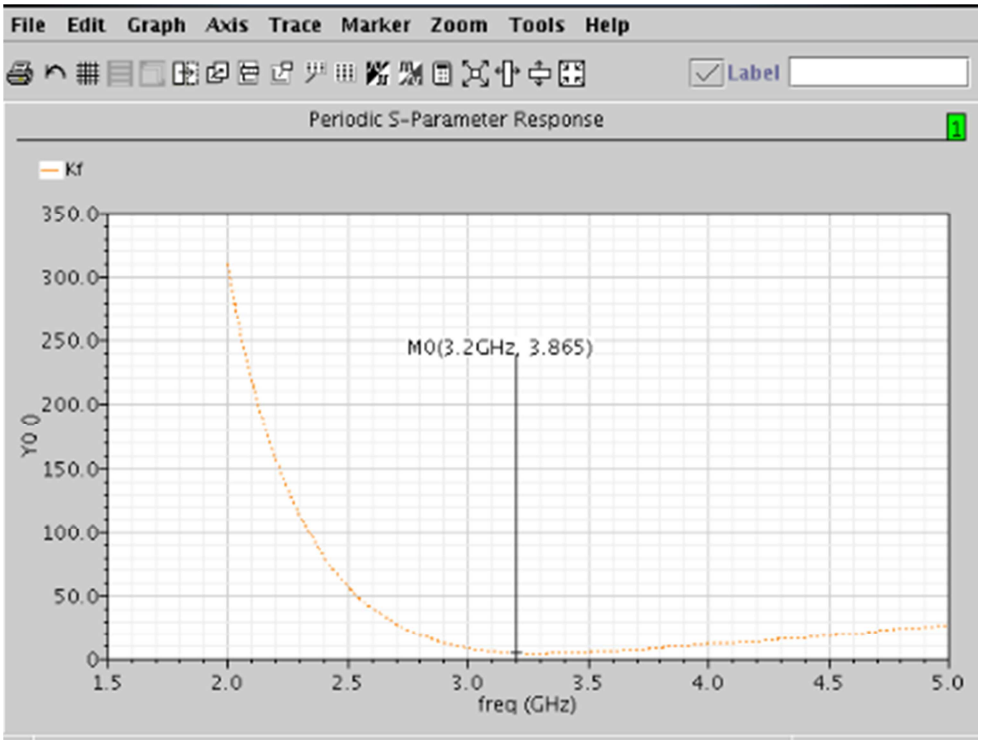

Figure 18. Values of the stability factor (KF).

Figure 19 illustrates the relation between the power added efficiency (PAE) and the input power at 3.2GHz where the PAE equals 12%, 39.5%, 47%, at -10dBm, -5dBm, 0dBm. These are good values of PAE.

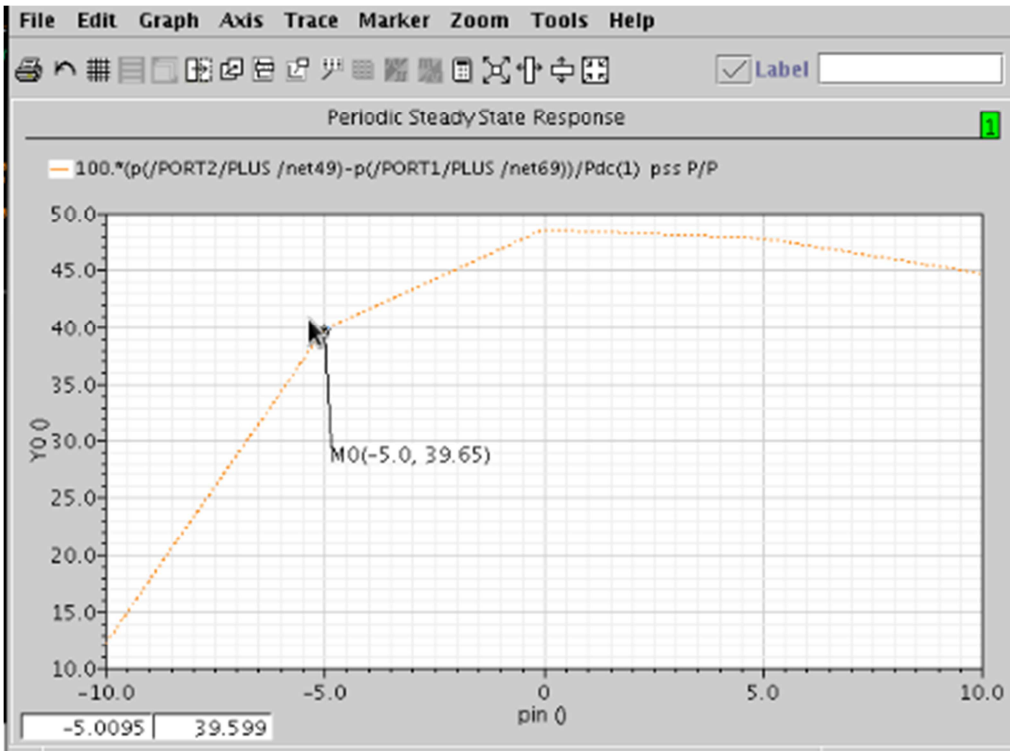

Figure 19. The power added efficiency (PAE) and input power.

5.1.3. Linearity of the CS PA

The linearity is measured with 1dB method shown in figure 20 for the input and in figure 21 for the output. Input Referred 1dB is about -4.7, Output Referred 1dB is about 14 at 3.2GHz.

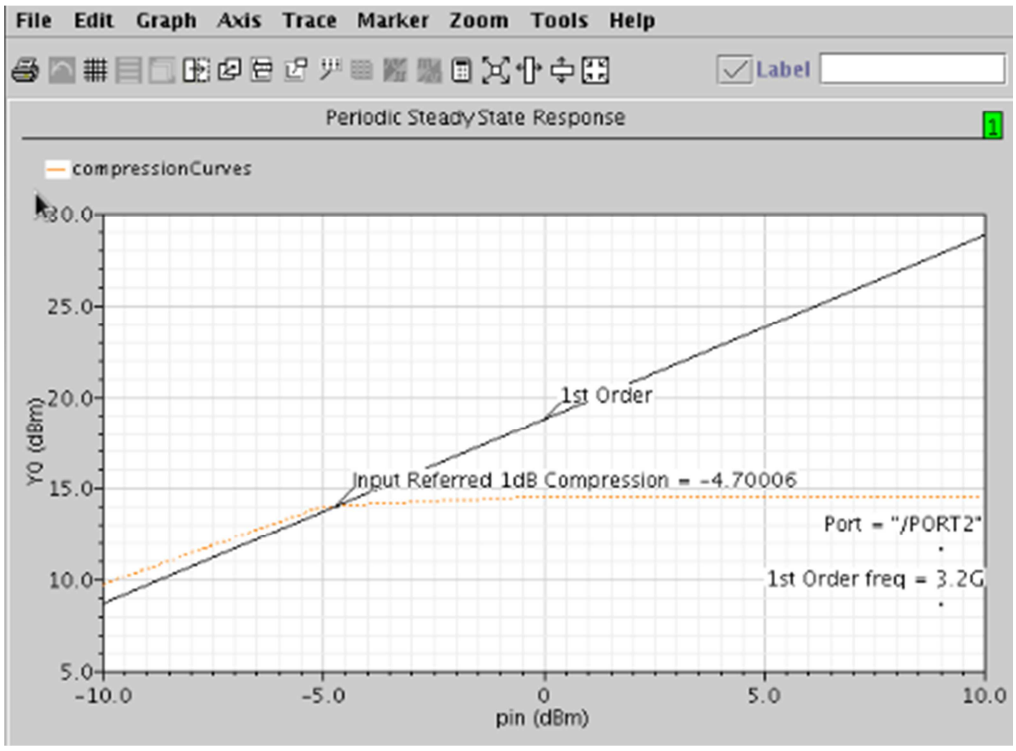

Figure 20. The Input Referred 1dB and input power.

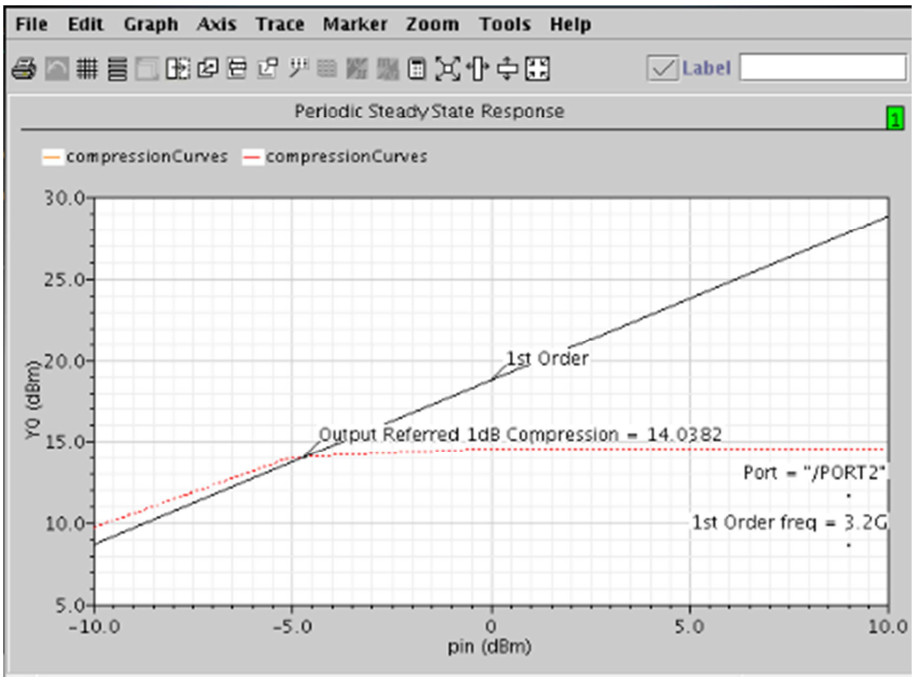

Figure 21. The Output Referred 1dB and input power.

5.2. Simulation Results for CS PA with DS

5.2.1. S Parameter

The PA is designed using TSMC 0.18µm technology. The simulation is achieved using Cadence and based on the device models provided by this technology. This PA operates at 2.2 to 5GHz under 1.8V voltage supply. Figure 22 shows the acattering functions S11, S12, S21, S22 respectively. From the figure it is seen that these functions have good values in the given frequency range. Table 2 shows the value of scattering functions at different frequencies.

Table 2. The value of scattering functions at different frequency.

requency	S11	S12	S21	S22
2.2 GHz	-1.77 dB	-66.7 dB	15.36 dB	-14.5 dB
3.2 GHz	-1.67 dB	-50.7 dB	27.19 dB	-2.6 dB
4.2 GHz	-2.9 dB	-51.5 dB	20.24 dB	-6.5 dB
5.0 GHz	-3.1 dB	-51.8 dB	16.2 dB	-9.5 dB

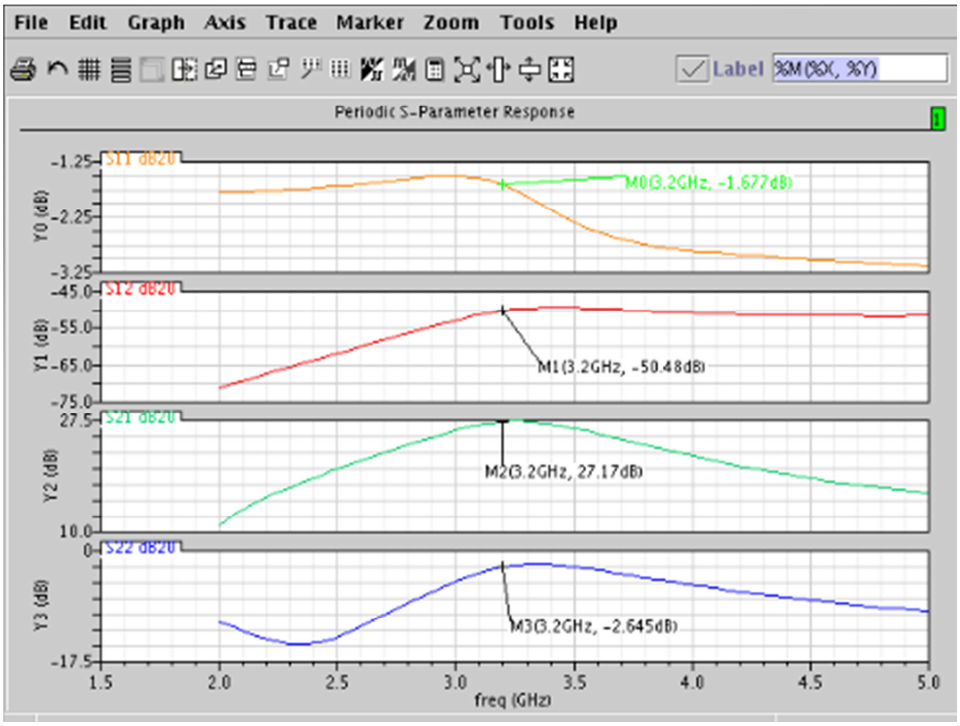

Figure 22. The scattering functions S11, S12, S21, and S22.

5.2.2. Stability Analysis of the CS PA with DS

The S-parameter simulation is used to measure stability of a transistor by the stability factor (KF) where its value should be more than one. Figure 23 shows the stability factor (KF) with a very good value of 7.2 at 3.2GHz.

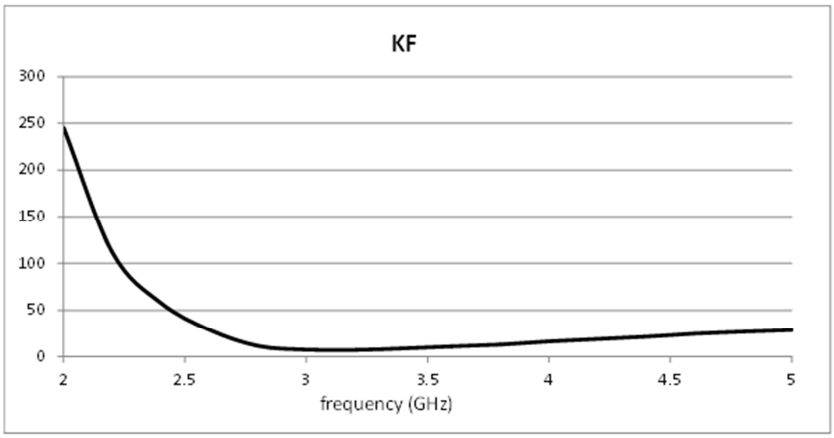

Figure 23. Values of the stability factor (KF).

Figure 24 illustrates the relationship between the power added efficiency (PAE) and the input power at 3.2GHz where the PAE equals 43.5%, 47.5%, 48%, at -10dBm, -5dBm, 0dBm. This shows good values to the PAE.

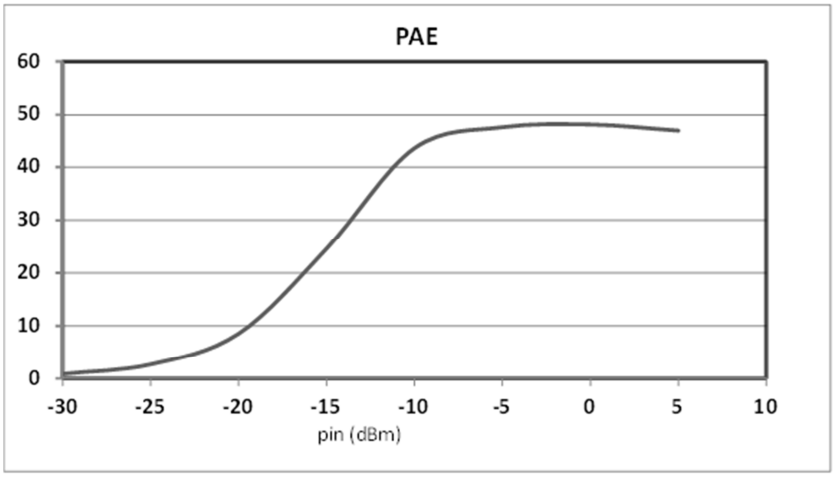

Figure 24. The Power added efficiency (PAE) and input power.

Figure 25 illustrates the relationship between the power added efficiency (PAE) and input frequency at input power -5dBm where the PAE equals 40%, 46%, 47.5%, 46.5% at 2.6GHz, 3GHz, 3.2GHz, 3.6GHz. This shows very good values to the PAE.

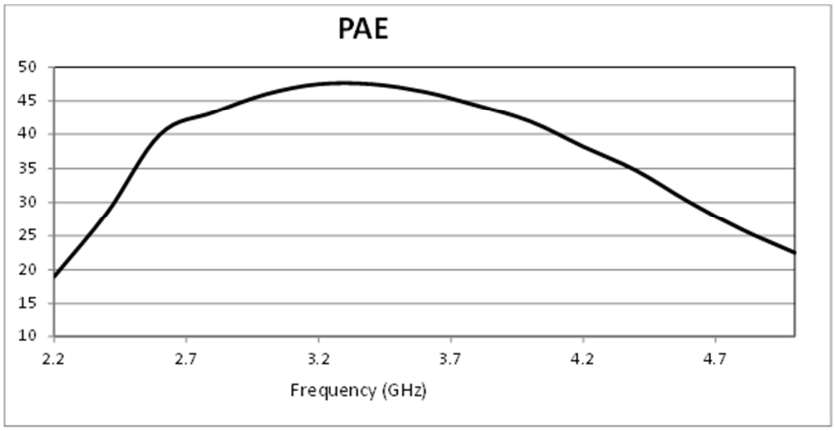

Figure 25. The Power added efficiency (PAE) and input frequency.

5.2.3. Linearity of the CS PA

The linearity is measured with 1dB method shown in figure 26. The Input Referred 1dB is about -14.6 and the Output Referred 1dB is about 12.9 at 3.2GHz. Figure 27 and figure 28 show the Input Referred 1 dB and the Output Referred 1 dB respectively. Notice that in figure 27, The Input Referred 1dB at input power -5dBm and the Output Referred 1 dB at

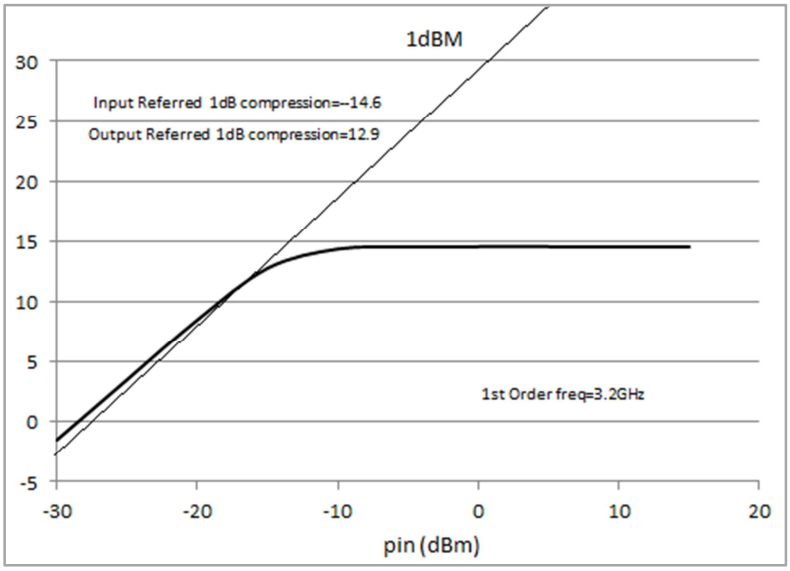

Figure 26. The Input Referred 1dB at input power -5dBm.

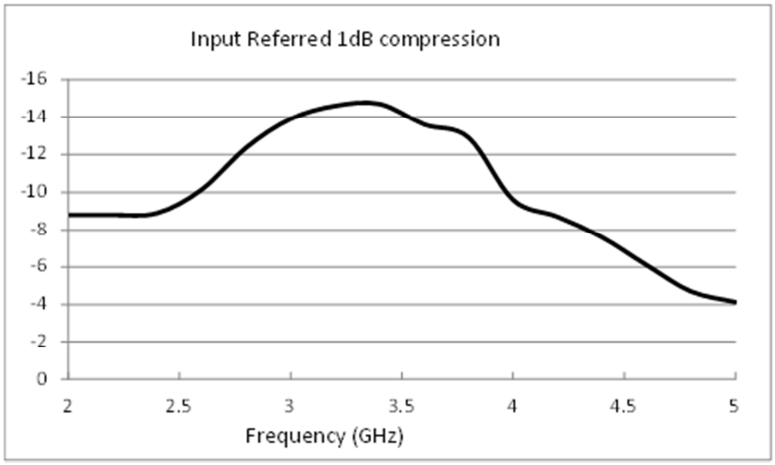

Figure 27. The Input Referred 1dB compression and frequency.

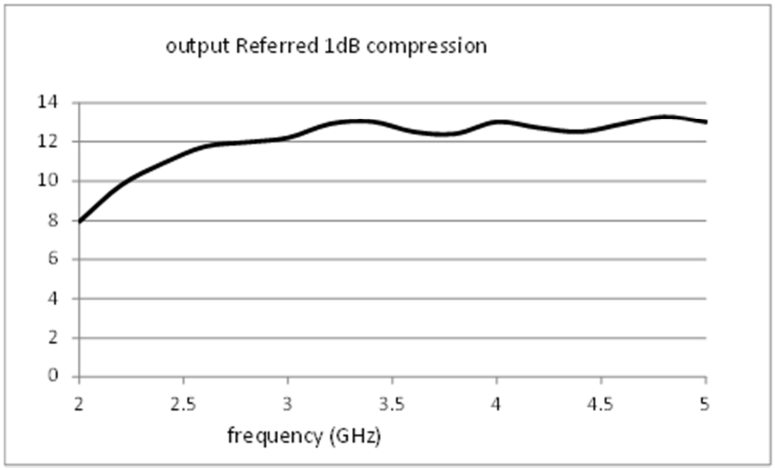

Figure 28. The Output Referred 1dB compression and frequency.

6. Discussion and Comparison with the Previous Work

To be able to evaluate the obtained results, they are compared with the results of other previous research. Table 3 presents this comparison. It can be seen from the table that the power obtained from the amplifier designed in this paper is 83.8 mw which is almost equal to the one obtained by Lu et al. [4] and both are the largest among the given research. However, the present results are much better than the other research results with respect to the PAE which is 47.5% in the present case and it is the largest efficiency among the given research results. The gain in the present paper is 27.19 which is less than the gain obtained by Vu et al. [11] which is 37.7 but still the present results are better because the efficiency obtained by Vu et al. [11] is 24.5%. Also, the parameters S11 and S22 are found in the present case to be much less than the corresponding values in the other research results.

7. Conclusions

This paper presented the most important parameters that define an RF Power Amplifier which are: Output Power, Gain, Linearity, Stability, DC supply voltage, Efficiency, Ruggedness. This paper presented these factors as well as the different classes of power amplifier. It presented the design and simulation of the Common Source Power Amplifier and then the Common Source Power Amplifier with derivative superposition (CS PA with DS) design method in the range of (2.2 – 5.0) GHz. To be able to evaluate the present results, the paper compared the results with the results of other previous research. The power obtained from the amplifier designed in this paper is 83.8 mw which is one of the largest values among the previous research. Although the obtained power is high, the other factors of the power amplifier are not affected. However, the paper results are much better than the other research results with respect to the PAE which is 47.5% in the present case and this is the largest efficiency among the given research results. The gain in the present case is 27.19 which is less than a previous work result which is 37.7 but still the present results are better because efficiency in that work is 24.5%. Also, the parameters S11 and S22 are found in the present case to be much less than the corresponding values in the other research results.

Table 3. Relationship of wideband CMOS PA performances: available and the present work.

Ref.	3dB BW (GHz)	S_{11} (dB)	S_{22} (dB)	Gain (dB)	P_{1dB} (dBm)	PAE (%)	Power (mW)
[3]	3 to 7	<-5	<-4	13 ± 1	+5 (output)	13%	21
[4]	3 to 12	<-10	<-8	10.46	+5.6 (output)	N/A	84
[9]	2.6 to 5.4	<-5	<-6	15.8	−3.4 (input) +11.4 (output)	34%	25
[10]	2 to 3	N/A	N/A	15.8 ±.0.1	+20.03 (output)	22%	N/A
[11]	2.4 to 2.48	<-18	<-15	37.7	−24.5 (input)	24.5%	N/A
[12]	3.1 to 4.8	<-10	<-8	19	−22.0 (input) −4.2 (output)	N/A	25
[13]	3.1 to 10.6	<-9	<-8	15	0 (output)	N/A	25.2
[14]	3 to 4.6	<-10	<-10	17.5	+0.42 (output)	3.9%	N/A
[15]	2.9 to 5.2	<-5.7	<-5.5	22.3	−11.5 (input) +9.8 (output)	26%	25
This work	2.2 to 5	<-1.67	<-2.6	27.19	−12.9 (input) +14.6 (output)	47.5%	83.8

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