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Step Response Analysis on First Order RC Circuit

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Abstract

Many details on the properties of a circuit can be determined by the step response. It is very important to know how a circuit responds to a sudden input. Fast deviations from the constant state might cause extreme effects on the component or on the system dependent on it. The step response provides information on the stability and ability to reach one constant state from another. In this paper analysis is done on the step response of a first order RC circuit. When time is 200μs the maximum output voltage received is 11.8144 and ratio is 82.3566.

Keywords

RC Circuit, Spice, Step Response, Transient Analysis

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1. Introduction

Capacitors store energy and it is important to determine the voltages and currents that arise in RC circuits, when the energy is gathered or released by the capacitor due to the sudden change in the DC voltage or current in the circuit. A capacitor consists of conductor pair separated by a dielectric. When a potential difference arises across the conductors an electric field is formed in the dielectric. This field stores the energy and makes a mechanical force between the conductors. The effect will be more when there is a narrow separation between large areas of the conductors [1]. Since capacitors store energy in the form of an electric field, they act like small cell which is able to store and release the electrical energy. A charge imbalance is caused between the two plates of capacitor on charging, which creates a reverse voltage as the capacitor becomes fully charged. When the capacitor is fully charged the current flow stops.

A capacitor when charged maintains a steady quantity of voltage across its terminals. A capacitor which is totally discharged, acts as a short circuit when it is attached to a voltage source, there by drawing the maximum current as it begins to charge. When the capacitor's voltage raises to the applied source voltage the current through the capacitor starts to decrease. On reaching the full source voltage, the drawing of current is stopped and it now behaves as an open circuit. When voltage source is applied to the RC circuit, the voltages and currents in the resistor and capacitor adjusts to the new conditions [2]. The current through the circuit is determined by the voltage difference between the source and capacitor, divided by the resistor used. If the change is a sudden step then the response of the voltages and currents is known as step response.

The step response provides many details on the properties of the circuit. It is the zero state response of a circuit when unit step input is applied to it. In the RC circuit as long as there is a potential difference across the resistor, the current will continue to flow. At the time when the capacitor voltage becomes equal to the source voltage, the voltage across the resistor will become zero and current will also fall to zero [3]. This will be the final state of the RC circuit. Thus the capacitor voltage rises from zero to the full source voltage whereas the current goes from maximum to zero. Both the variables changes and approaches their final values with time. For a linear time invariant circuit, when the input

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source function gets integrated the zero state response also gets integrated. The integral of unit impulse function will be the unit step function. Thus the step response will be the integral of the impulse response.

To change the voltage by a not zero finite amount instantaneously, an impulse current flow through the capacitor. The step response analysis provides the concepts of natural, forced, zero input and zero state responses. The zero state responses contain steady state response term and transient term. The steady state current in a series RC circuit will be zero, which shows that the energy flow from the source occurs only during the charging process [4, 7]. No energy will be drained from the source when the capacitor is fully charged.

For finding the optimum design of a circuit, transient and steady state excitations helps a lot. The transient period lies between the initial and the final state, when the voltage and current adjust to new conditions caused by the voltage source.

When the capacitor initial voltage is zero and the input voltage applied is a step function of magnitude V, then

$$V(t) = \begin{cases} V & t \geq 0 \\ 0 & t < 0 \end{cases} = V\,u(t) \qquad (1)$$

The step response form

$$Vc^{(step)}(t) = [\, V_o e^{-t/RC} + V\,(1 - e^{-t/RC}) \,]\, u(t) \qquad (2)$$

When the capacitor is initially uncharged

$$Vc(t) = V\,(1 - e^{-t/RC})u(t) \qquad (3)$$

The initial capacitor voltage is zero which rises in a monotone manner till it reaches a steady voltage of V volts. The RC time constant determines the rate at which $Vc^{(step)}(t)$ approaches the steady state voltage. Natural response shows the solution when input is zero. When the input is step function, it forms the forced response. The step response reaches to its final value after approximately five time constants [5]. In this paper simulation is done on first order RC circuit using linear technology spice software to analysis its step response. The output is analyzed for the time when R1*C1 is 200µs.

2. Research Methodology

The first order RC circuit is drawn using linear technology spice software as shown in figure 1. The resistor value is selected at 1.2 kilo ohm and capacitor at 100 nano farad. In/Out labels are marked at the nodes and ground terminal is connected to the circuit. The independent voltage source is selected with the function set to none and DC value of 12 V as shown in Figure 2.

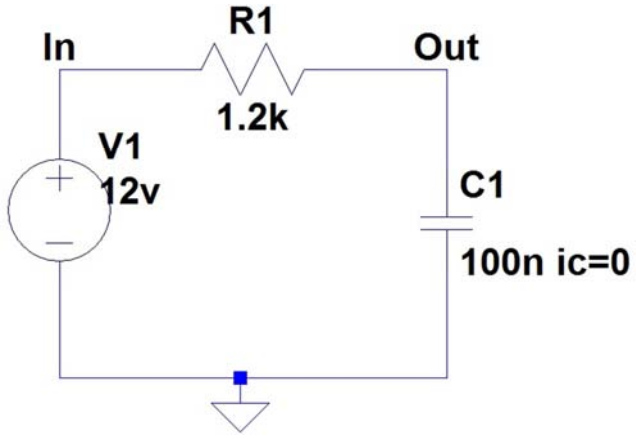

Figure 1. First order RC circuit.

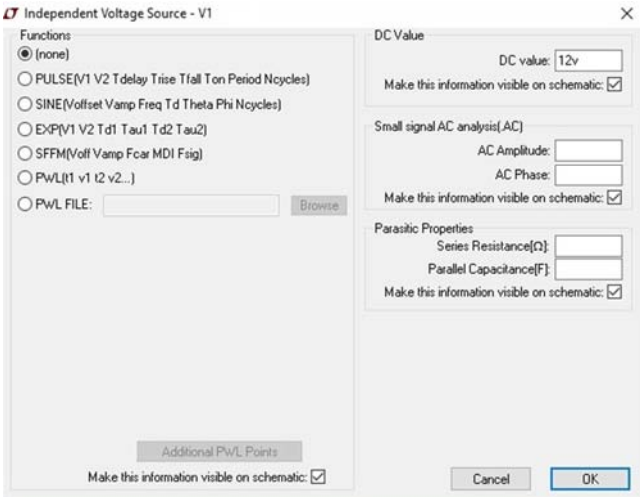

Figure 2. Independent voltage source.

The number of calculations required to plot a wave form is determined by the ratio of stop time and maximum time step. The probe screen will be cluttered with unnecessary points if the time step are kept very small, and also it will make the calculations time more. Whereas high time step will make the important process to be missed which occurs in very short periods of time in the circuit. Therefore a proper value must be maintained. In simulation, the time does not simply happen, one need to make it happen [6].

After setting the source, the transient analysis is then selected as shown in figure 3. The transient analysis depends on time. During transient analysis DC component of the source is applied to the circuit. It saves the node voltage and current in branches at each time point in the analysis. The stop time is selected 0.5ms, time to start saving data is kept at 0, and maximum time step is kept 0.01m. Start external DC supply voltages at 0V, stop simulating if steady state is detected and step the load current source box are left unchecked.

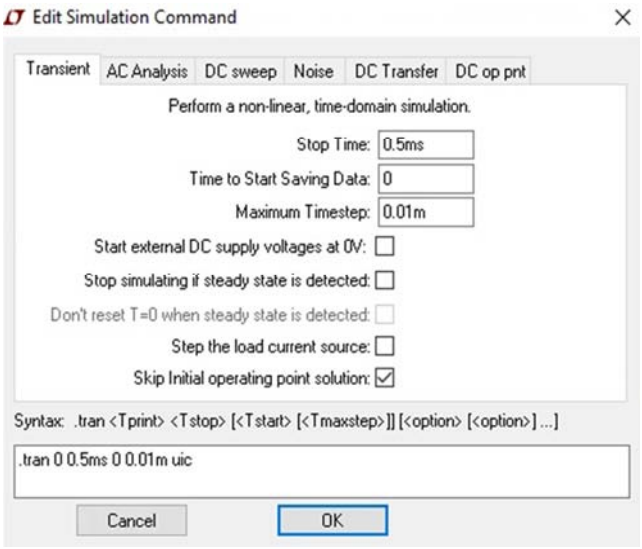

Figure 3. Transient analysis.

The simulation is run by selecting V (Out) from the add trace to plot option and the graph is formed as shown in figure 4. The maximum value of scale in X axis is 500µs and Y axis is 12 volt. From the graph, the V out at 250µs is 10.5038 volt.

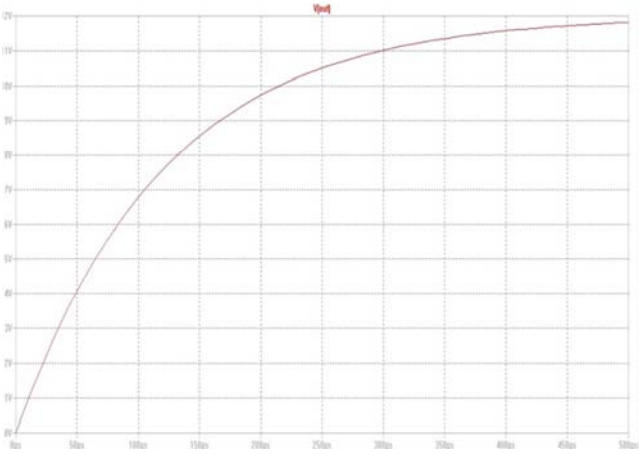

Figure 4. Output.

Now for the time = R1*C1=200µs the value of V(out) is calculated. Using the.op the directive [.meas tran vrc find v(out) AT=200µ] is added to the circuit. In the syntax tran is the measure on the result by transient analysis, vrc is the user defined parameters which receives the result, v(out) is the output voltage on which measure is done and AT=200u is the time at 200µs. The transient analysis computes the happenings when the circuit is powered up. It starts at the time equal to zero. The data between zero and T start will not be saved if T start is specified. It allows managing the size of the waveform by ignoring startup transients. According to the need various modifiers can be placed on the tran line.

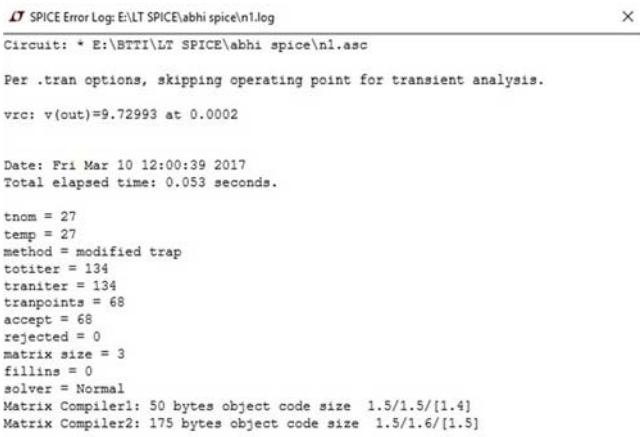

Figure 5. Error Log 1.

From the view tab, the spice error log is selected as shown in figure 5. Vrc shows the value of v(out) at t=200µs. To find the step response of a first order RC circuit the initial value, final value and the time constant are required. For t>5Tc the step response reaches a constant DC value [7]. The capacitor acts like an open circuit under the DC conditions [8].

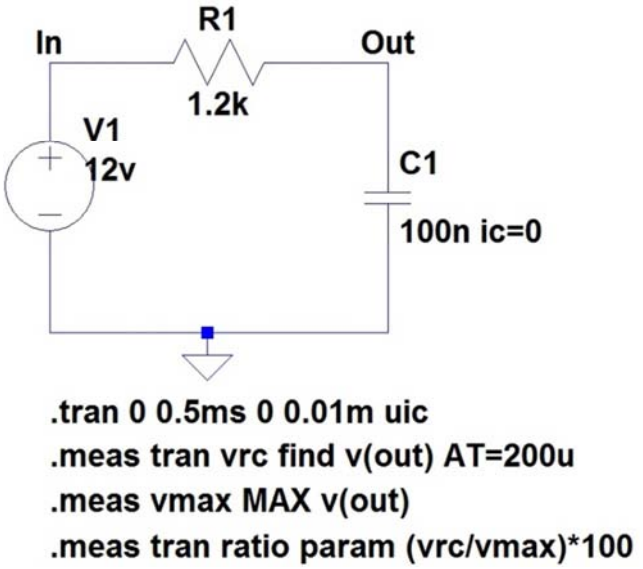

Figure 6. Modified circuit with parameters.

Now the circuit is modified with the parameters as shown in the figure 6. The syntax [.meas vmax MAX v(out)] and [.meas tran ratio param (vrc/vmax)*100] is added. Measure statements are very useful in evaluating user defined electrical quantities. In LT spice there are two types of meas statements. First statement refers to a point along the abscissa and is used to print a data value or expression at a specific point or when a condition is met. It is possible to state the type of analysis to which the meas statement applies. This makes to apply certain meas statements only for certain type of analysis. If ordinate information is not requested then the meas statement prints point on the abscissa.

The second statement refers to a range over the abscissa. It is specified with the points defined by trig and trag. If the points are omitted then the meas statement operates over the entire range of data. After the simulation is completed, meas statements are done in post processing [9]. The param directive allows creating user defined variables. It helps in associating a name with a value so that abstract circuits can be saved in libraries. To limit the scope of the parameter value, the param statement can be included inside a sub circuit definition. When the expression is enclosed in curly braces it will be replaced with the floating point value. The parameters will not pass to the sub circuit as an evaluated value. The expression is evaluated on the basis of all relations and reduced to a floating point value, when the curly braces are encountered. Before the beginning of simulation all the parameter substitution evaluation is finished.

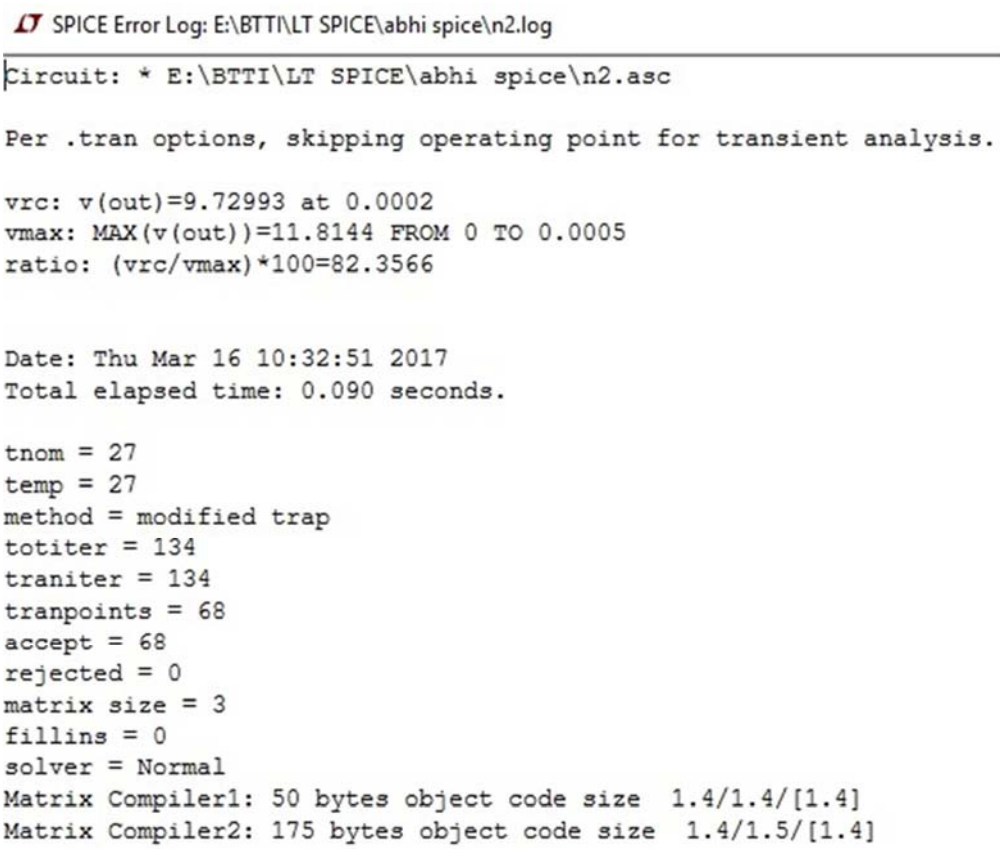

Figure 7. Error Log 2.

In the RC circuit as the voltage of capacitor increases the voltage across resistor decreases. It makes the charging current down in a decreasing rate. During the charging process there will be an energy flow from the DC source and when the capacitor is fully charged energy will not be drained from the source [10]. Now the simulation is run and on selecting the spice error log, Max Vout and ratio is received as shown in figure 7.

3. Conclusion

The transient and steady state excitations greatly help in finding the optimum design of a circuit. Approximately after five time constants the step response reaches to its final value. Analysis is done on the step response of a RC circuit and for the time R1*C1=200µs the value of output voltage is calculated which was found to be 9.72993. The input DC voltage source is selected at the value of 12 V. The Max Vout received is 11.8144 and ratio is 82.3566.

By changing the value of resistor and capacitor various effects on the step response of a first order RC circuit can be seen. The step response of a system thus gives vital information on the stability and ability to reach one stable state when starting from another. A system is unable to act until the output of its component settles down to its final state, which will delay the overall response of the system. With respect to the time of the impulse response the step response is an integral. The findings of this research will help the designers to avoid adverse extreme effects on the component or on the system dependent on it.

References

[1] Alexander L. Schulz. Capacitors: Theory, Types, and Applications. Nova Science Publishers, pp 18, 2010.

[2] Mahmood Nahvi, Joseph A. Edminister. Schaum's Outline of Electric Circuits. McGraw-Hill, pp 318, 2014.

[3] James William Nilsson, Susan Riedel. Electric Circuits, Pearson, pp 266-269, 2008.

[4] K. S. Suresh Kumar. Electric Circuits and Networks, Pearson, pp 420-421, 2008.

[5] Oktay Alkin. Signals and Systems, CRC press, pp 148-150, 2014.

[6] Francois E. Cellier, Ernesto Kofman. Continuous System Simulation. Springer, pp 11-12, 2006.

[7] Roland E. Thomas, Albert J. Rosa, Gregory J. Toussaint. The Analysis and Design of Linear Circuits, John Wiley & Sons, pp 321-322, 2012.

[8] Cletus J. Kaiser. The Capacitor Handbook A Comprehensive Guide For Correct Component Selection In All Circuit Applications. C J Publishing, 2 edition, pp 77, 2011.

[9] Gilles Brocard. The LTSpice IV Simulator Manual, Methods and Applications, Swiridoff Verlag, pp 316, 2013.

[10] R. P. Deshpande. Capacitors, Tata McGraw Hill, pp186, 2014.

Biography

Mr. Abilash is involved in R&D with various research papers in AJMIE, MSIMJ, IJSRD, IJRASET, IJTRE, IRJET, IJNN, IJAEAS, IJAPST and SIIJ. He did MTech, BTech, IE, IA, DBME, SAHC, CSHAM, FPM, IEEE-(MT, NESC), IIT-(ETFET, TCSE, 3DAV, PFEUIST), ITP and IPD. He participated in various conferences and seminars like RACSIP-IETE, NT-CNTR VIT, RMET-IIT Bombay, FPGA-Bangkok University, MDE-ENSISA-UHA France, LT Spice-IUT Angouleme France and TDP-EF Zurich.

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